Voltage Controlled Differential Ring Oscillator Based on the SCFL Delay Cell

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Abstract - This paper describes the simulations performed in order to evaluate expected performance of the voltage-controlled oscillator (VCO) based on differential ring oscillator with SCFL delay cells in 0.5-μm GaAs MESFET technology. The ring oscillator structures with buffer cells are also simulated. The frequency range and tuning sensitivity are extracted. Finally, jitter simulations are performed in order to assess the sensitivity of various VCO configurations to the power supply variations.

I. INTRODUCTION

One of the well-known GaAs families is source-coupled FET logic (SCFL) [1,2]. It dissipates more power than the direct-coupled FET logic family (DCFL), however it is very fast, well suited to the implementation of complex gates and tolerant to technology variations because of the usage of differential inputs.

Many modern, high-speed, high-performance integrated circuits require a low-phase-noise (low-jitter) clock that operates in the GHz range. Fabricated on the same substrate as the rest of the circuit, the phase-locked loops (PLL) or frequency synthesizers must typically operate from the global supply and ground busses, thus experiencing both substrate and supply noise. In time domain noise manifests itself as jitter of the output voltage, primarily through various mechanisms in the voltage-controlled oscillators [3,4].

Power supply variations of the VCO change the delay of each stage inside the VCO. If a VCO has nonideal power supply rejection, it is likely that the delay of each delay cell is linearly proportional to change in the power supply. High-frequency supply noise couples into the VCO and periodic supply noise generates delay variations of the delay stages inside the VCO [5]. It is possible to reduce jitter by separating supply of the VCO from the rest of the circuit [5].

Due to their high operating frequency and ease of integration, use of ring oscillators in jitter sensitive applications is becoming more common [6]. Generally, the phase noise of a single-ended oscillator is smaller then the phase noise of the differential ring oscillator. However, differential ring oscillators are less affected by supply and substrate noise [7].

In this paper we consider differential ring oscillators consisting of SCFL delay cells. Section II describes various differential ring oscillator structures and their performance in terms of the oscillator frequency, amplitude and tuning sensitivity. Section III presents jitter definitions and simulation results for the period jitter and adjacent period jitter, while Section IV gives conclusions.

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II. DIFFERENTIAL RING OSCILLATOR

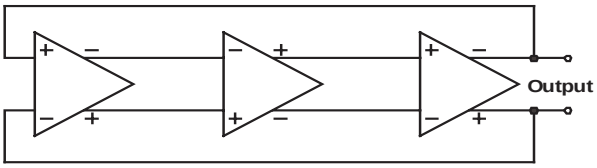

Fig. 1. Differential ring oscillator (DRO) consisting of three cells.

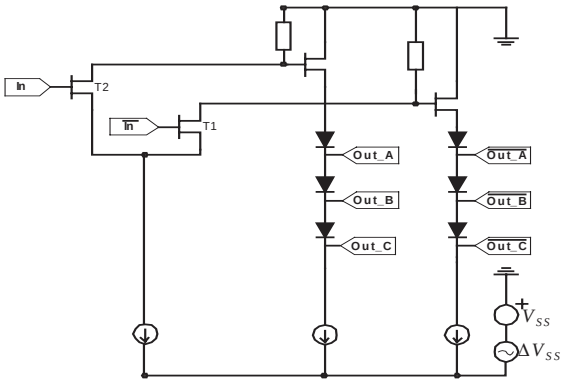

Fig. 2. SCFL buffer cell.

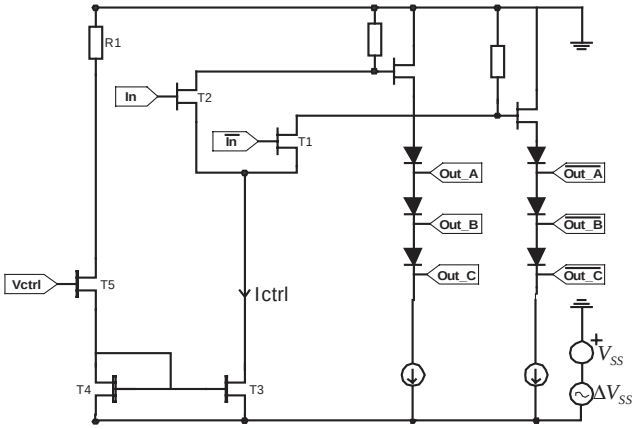

Fig .3. Voltage controlled SCFL delay cell.

Fig. 1 shows a three-stage ring oscillator where signal path is differential in order to achieve high common-mode rejection. Fig. 2 shows an SCFL buffer cell used as the inverter in the differential ring oscillator. The voltage source ΔV_{SS} in Fig. 2 and 3 represents the supply noise and

is modeled here by a sinusoid with the frequency 250 MHz or 500 MHz and amplitude of 100 mV.

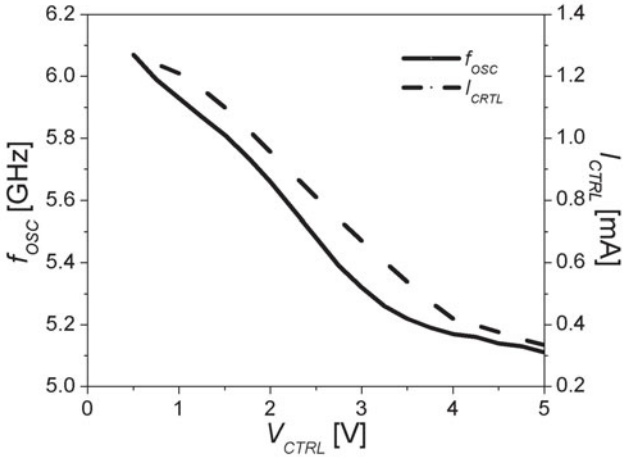

Fig. 4. Frequency of oscillation f_{OSC} and current I_{CTRL} vs. control voltage V_{CTRL} (VCDRO with 3 SCFL delay cells).

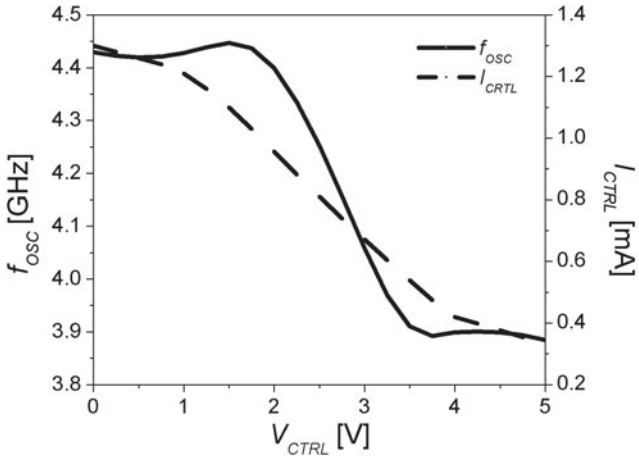

Fig. 5. Frequency of oscillation f_{OSC} and current I_{CTRL} vs. control voltage V_{CTRL} (VCDRO with 4 SCFL delay cells).

Table 1. Influence of varying VCDRO parameters and varying the number of cells in VCDRO on frequency of oscillation and tuning sensitivity (N).

Number of cells in VCDRO N	Frequency of oscillation f_{OSC} [GHz]	Tuning sensitivity K [MHz/V]
3	5.11-6.07	230
4	3.91-4.45	275

The frequency of oscillation f_{OSC} of the ring oscillator with N cells can be approximated by

$$f_{OSC} = \frac{1}{2 \cdot N \cdot t_d} \qquad (1)$$

where t_d is the delay of each cell.

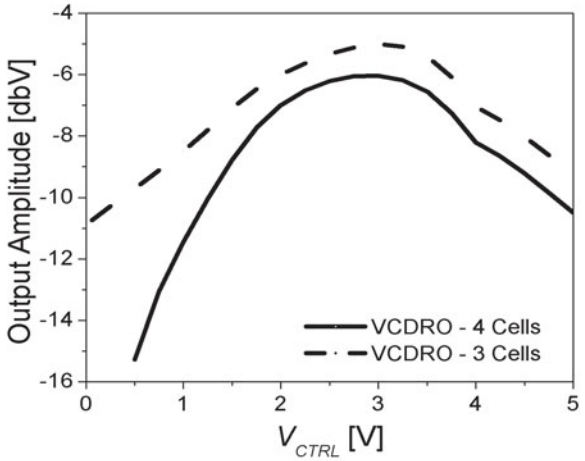

Fig.6. Amplitude of the first harmonic of the output signal vs. V_{CTRL}.

By varying time delay t_d of each cell in the ring oscillator we are able to change frequency of oscillation. This is accomplished by varying the current I_{ctrl} through differential pair of transistors (*T1* and *T2*) in Fig. 3, which changes the delay time of the cell. The current I_{ctrl} is set by current mirror (*T3* and *T4*) and controlled with the transistor *T5* and resistor *R1*.

Voltage controlled SCFL delay cell has 3 outputs (*Out_A*, *Out_B*, *Out_C*), shifted approximately 0.7 V to each other, their complements, and therefore it can be used with any other standard SCFL cell in this technology. Connecting an odd number of voltage controlled SCFL delay cells (as invertors) produces the voltage controlled differential ring oscillator (VCDRO).

The differential ring oscillator (DRO) shown in Fig. 1, realized with SCFL buffer cell in Fig.2 and VCDRO, realized with SCFL delay cell are simulated with the SPICE parameters for the 0.5-μm GaAs MESFET process [8]. Figs 4 and 5 show the frequency of oscillation f_{OSC} and the control current I_{CTRL} for the 3- and 4-stage VCDRO, respectively, as a function of the control voltage V_{CTRL}. The frequency varies from 6.07 GHz to 5.11 GHz as the control voltage is varied from 0.5 V to 5 V in the case of the 3-stage VCDRO, and from 4.45 GHz to 3.91 GHz in the case of the 4-stage VCDRO. Table I also shows the tuning sensitivity of these VCDROs.

Figure 6 shows the amplitude of the output signal (first harmonic) as a function of control voltage $V_{CTRL.}$ The highest peak-to-peak amplitude is obtained at $V_{CTRL} \cong 3V$, which corresponds to $f_{OSC} \cong 4$ GHz for the 4-stage VCDRO and $f_{OSC} \cong 5.3$ GHz for the 3-stage VCDRO.

Note that the 4-stage VCDRO has narrower useful range of the control voltage. This is a result of the usage of the same delay cell in both VCDRO configurations. The cell is easily modifiable and the useful control voltage sweep may be easily adjusted to the full 5V range.

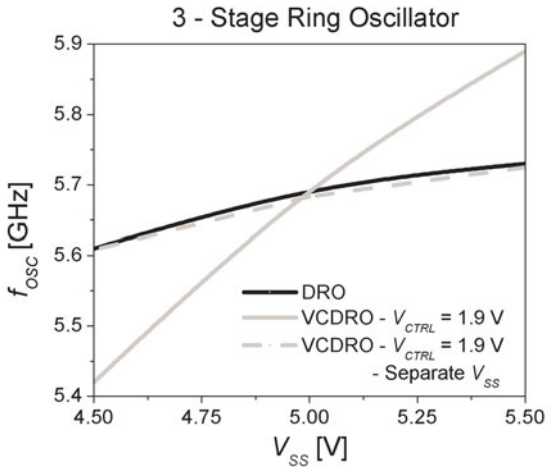

Fig. 7. Frequency of oscillation f_{OSC} vs. V_{SS} for differential ring oscillator with three 4 mW invertors (DRO) and differential ring oscillator with three voltage controlled SCFL delay cells (VCDRO) with and without separate V_{SS} for the current mirror in SCFL delay cell.

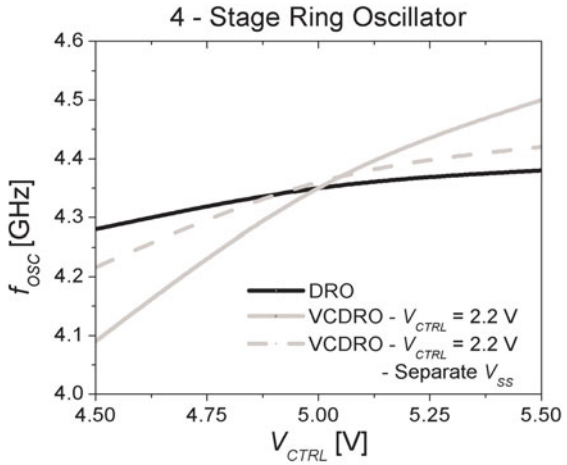

Fig. 8. Frequency of oscillation f_{OSC} vs. V_{SS} for differential ring oscillator with four 4 mW invertors (DRO) and differential ring oscillator with four voltage controlled SCFL delay cells (VCDRO) with and without separate V_{SS} for the current mirror in SCFL delay cell.

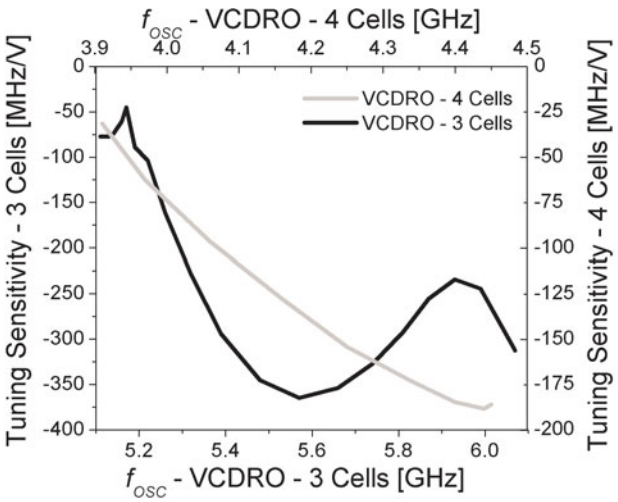

Fig. 9. Tuning sensitivity as a function of the oscillator frequency.

The influence of the power supply variation (±10% of V_{SS}) is shown in Figs. 7 and 8. VCDRO is more influenced by power supply variation then DRO because the current I_{CTRL} that affects t_d is also changed by changing power supply voltage. This effect can be suppressed by separate filtered and stabilized power supply for the current mirror in the SCFL delay cell.

Fig. 9 shows tuning sensitivity of a 3- and 4-stage VCDRO.

III. JITTER AND PHASE NOISE ANALYSIS

Jitter is generally defined as short-term, non-cumulative variation of the significant instant of a digital signal from its ideal position in time.

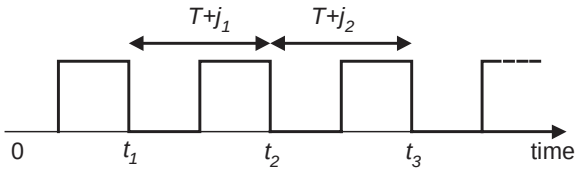

Fig. 10. Clock signal with transition-time jitter.

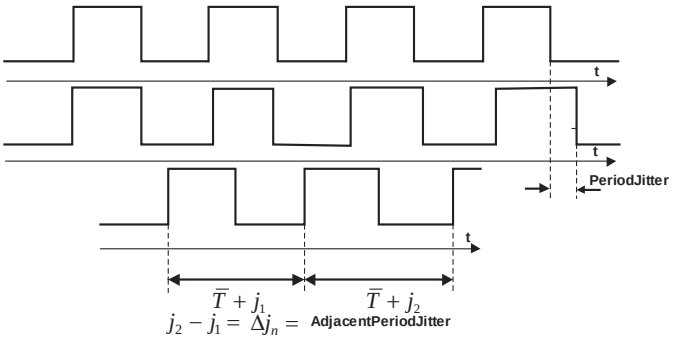

Fig. 11. Period jitter and adjacent period jitter.

Suppose $\{t_n\}$ is a sequence of transition times from a clock with nominal period T (Fig. 10). The sequence

$$\{t_n\text{-}nT\} \quad (2)$$

characterizes absolute jitter [9]. Absolute jitter is also used to describe the tracking error between two clocks.

The sequence

$$\{j_n := t_{n+1} - t_n - T\} \quad (3)$$

characterizes the variation in the period from the nominal period (Fig. 11). Commonly known as period jitter (PJ) [9], this is also called cycle jitter in [3, 4], edge-to-edge jitter and cycle-to-cycle jitter.

It is also possible to define jitter over k periods by

$$\{j_n(kT) := t_{n+k} - t_n - kT\} \quad (4)$$

which is sometimes referred to as long-term jitter.

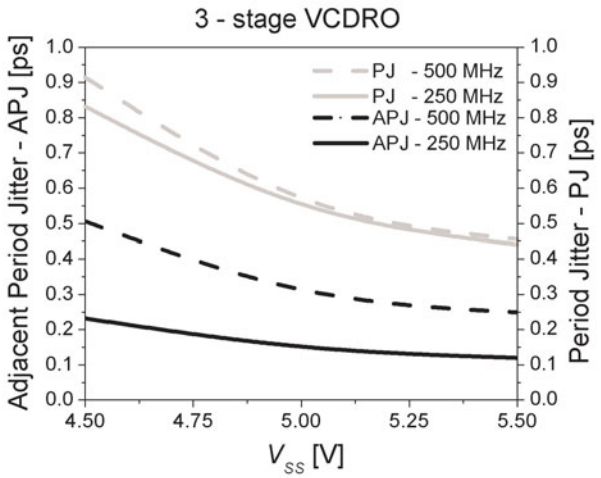

Fig. 12. Standard deviation of period jitter (PJ) and adjacent jitter (APJ) of a 3-stage VCDRO output vs. power supply voltage, when power supply noise is modeled with 250 MHz and 500 MHz sinusoid (100 mV peak amplitude).

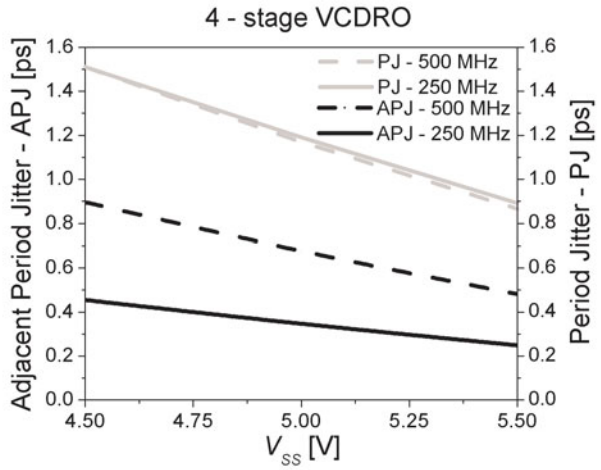

Fig. 13. Standard deviation of period jitter (PJ) and adjacent period jitter (APJ) of a 4-stage VCDRO output vs. power supply voltage, when power supply noise is modeled with 250 MHz and 500 MHz sinusoid (100 mV peak amplitude).

Another common measure of jitter is adjacent period jitter (APJ) [9],

$$\{\Delta j_n := j_{n+1} - j_n = (t_{n+2} - t_{n+1}) - (t_{n+1} - t_n)\} \quad (5)$$

shown in Fig. 11. This is also called cycle-to-cycle jitter in [3,4].

Figures 12 and 13 show standard deviation of the period jitter and adjacent period jitter for the ring oscillators consisting of 3 and 4 SCFL delay cells, respectively. The standard deviation is obtained by

$$\sigma = \sqrt{\frac{\sum_{i=1}^{M}(x - \bar{x})^2}{M-1}} \quad (6)$$

on a sample of M elements, where x represents data (APJ or PJ) and $\bar{x}$ represents mean value of sample.

In contrast to the single-ended ring oscillator, a differential ring oscillator does exhibit a phase noise and jitter dependency on the number of stages with the degradation of the phase noise as the number of stages increases for a given frequency and power dissipation [7].

IV. CONCLUSION

This paper describes the simulations performed in order to evaluate expected performance of the voltage-controlled oscillator (VCO) based on differential ring oscillator with SCFL delay cells in 0.5-μm GaAs MESFET technology. The ring oscillator structures with buffer cells are also simulated. The frequency range and tuning sensitivity are extracted. Finally, jitter simulations are performed in order to assess the sensitivity of various VCO configurations to the power supply variations.

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