COMPARISON OF NON-LINEAR MESFET MODELS OVER 1-12 GHZ FREQUENCY RANGE[1]

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ABSTRACT

This paper is an extension of work done previously on the comparison of non-linear MESFET models [3]. The list of models that are compared includes the Curtice quadratic, Curtice cubic, Statz, Materka, and Advanced Materka models to which the Angelov's model has been added. Furthermore, measurements and model prediction of intermodulation distortion (IMD) are now extended to 12 GHz. The comparison is based on the relative error observed between the measured and simulated DC I-V data, and average error for the model prediction of high frequency gain and IMD. Performance of various models is discussed.

1. INTRODUCTION

GaAs MESFETs are used in a variety of high-frequency and non-linear applications and it is, therefore, very important to model their behavior accurately across a large frequency and bias range. Initial study of DC and ac performance of various models was done in [1] and for non-linear performance in [2]. Different empirical models have been built over the years and various factors, such as gain, are used in comparing the performances of these models. An additional figure of merit is the amount of intermodulation distortion (IMD), which shows the effects of non-linear interactions of signals applied to the device. IMD is also relatively straightforward to measure.

In this work we analyze six models: Curtice quadratic and cubic, Statz, Materka, Advanced Materka and recently added Angelov's model [3-5], which are evaluated across a wide frequency and bias range.

2. MESFET MODELS

The topology of the large-signal MESFET model is common to all the models being investigated, and is shown in Figure 1. The difference among the models is primarily in the functions that govern the current source I_{ds} and capacitances C_{gd} and C_{gs}.

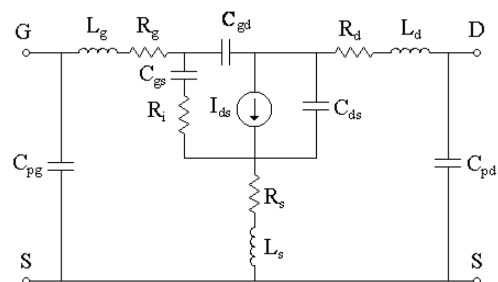

Figure 1. Large-signal model topology.

The extraction of various device parameters is often based on a small-signal equivalent circuit, which is some simplification of the large-signal model. Only the bias variation of different elements has to be modeled, typically by using a set of fitting formulas. The parameters for the formulas are extracted through an optimization procedure.

3. DC AND C-V MEASUREMENTS AND SIMULATIONS

The devices used for our measurements were on-wafer GaAs MESFETs with 300μm gate width. The results reported here were obtained from different devices and equipment than the results reported in [3] but the observed characteristics were, in general, very similar to our previous results. The DC measurements were done using HP 4145B parameter analyzer. The S-parameters were measured using Cascade ACP probes connected to Agilent 8722E vector network analyzer in the frequency range from 0.1 to 26.1 GHz. The DC and S-parameters were measured at the following bias points for parameter extraction: V_{ds} (drain voltage)=0V to 3V with a step of 0.2V and 3V to 8V with a step of 1V and V_{gs} (gate voltage)= -2.75V to 0.25V with a step of 0.25V. In addition, a set of "cold FET" measurements (V_{ds} = 0) was done.

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The model parameters were extracted using IC-CAP from Agilent [8]. All the models are built-in except for the Angelov's model, which was implemented on IC-CAP as a user defined model. The circuit simulations were carried out on Agilent ADS [9]. The Angelov's model is implemented on ADS using the Symbolically Defined Device (SDD) feature.

The extrinsic parameters R_D, R_G, R_S, L_D, L_G, L_S were obtained after the de-embedding using the procedure given by Dambrine [6]. These parameters are shown in Table 1 and are kept fixed in the subsequent steps.

Table 1. Parasitic resistances and inductances

Parasitics	Rd	Rg	Rs	Ld	Lg	Ls
Value	3.2 (Ω)	1.4 (Ω)	2.1 (Ω)	30.01 (pH)	26.08 (pH)	2.76 (pH)

The intrinsic MESFET parameters were obtained after the de-embedding procedure. The initial DC and C-V parameters were obtained through extraction routines in IC-CAP and typically involved optimization on a subset of measured data. These model parameters were then included into ADS models and were globally optimized by reducing the relative error between the measured and simulated data.

The relative error is used in comparing various DC models and it is calculated from the following:

$$\text{REL._Error} = \frac{\sum \left| \frac{SIMULATED_VALUE - MEASURED_VALUE}{MEASURED_VALUE} \right|}{NUMBER_OF_TESTPOINTS} \quad (1)$$

Relative error gives a better representation for errors for the smaller current values. Table 2 contains the average relative error for five gate voltages. Shaded numbers indicate the best result.

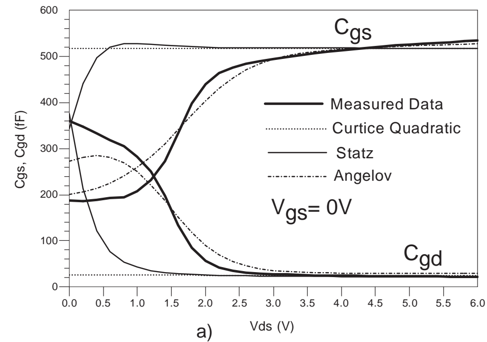
Table 2. Relative error for a set of output I-V curves; V_{ds} changes from 0V to 6V.

Vgs	Angelov's	Curtice quadratic	Statz
-2.0V	213.96%	256.76%	44.2%
-1.5V	11.03%	21.42%	13.9%
-1.0V	7.105%	8.74%	6.07%
-0.5V	5.96%	6.68%	5.17%
0V	6.95%	8.4%	7.81%

Vgs	Curtice cubic	Materka	Advanced Materka
-2.0V	**39.18%**	207.25%	100%
-1.5V	**7.3%**	25.14%	8.59%
-1.0V	**5.85%**	7.82%	5.87%
-0.5V	5.97%	6.74%	**5.16%**
0V	7.68%	7.77%	**6.46%**

The best fit is given by Curtice cubic and Advanced Materka, but the differences are not as pronounced as observed before [3]. The Angelov's model does not provide a good fit for gate voltages near cut-off. We observed somewhat increased knee voltage in the output I-V measurements, which made the accurate fit in the linear region more difficult, resulting in errors higher than previously observed. The source and ramifications of this increase in knee voltage are being investigated.

C_{gd} and C_{gs} were obtained by measuring S-parameters from 100MHz to 26.1GHz and by de-embedding the device so that intrinsic device parameters could be calculated. The C_{gd} and C_{gs} for a particular bias were obtained by averaging their values over the frequency range, but the actual variation of capacitances up to 10GHz was small. This procedure was repeated for V_{gs}= -2 to 0V in steps of 0.5V, with Vds swept from 0 to 6V for each V_{gs}. As illustrated in Figure 2, Angelov's model has the best fit to C-V measurements, especially at low values of V_{ds}. Zero bias capacitances were found to be C_{gd0}=23 fF, C_{gs0}=520 fF. In addition, f_T =20 GHz, and f_{max} > 40 GHz were deduced from S-parameters.



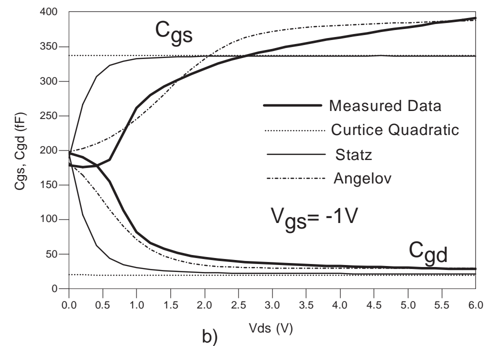


Figure 2. C-V measurements vs. simulation, a) V_{gs}=0V, b) V_{gs}=-1V.

4. INTERMODULATION DISTORTION

After the non-linear model parameters were extracted and optimized, we next investigated intermodulation distortion (IMD), which is a nonlinear effect occurring when two or more excitation frequencies are applied to the device. Output power is then distributed among the fundamental, second-, third-, fourth-, and higher-order IMD frequencies. In our experiments we applied two excitation frequencies, f_1 and f_2, separated by 1 MHz. Third-order IMD product (IMD3) will occur at $2f_1$-f_2 and

$2f_2$-f_1. Output power was measured at fundamental and IMD3 frequencies.

We measured IMD at 3 different biases and at eleven different center frequencies. Biases were chosen to represent low-noise, class A, and maximum gain region of operation. Table 3 shows the measurements made for 1.1 GHz. The other center frequency points are as follows: 1.4, 1.7, 2.3, 2.6, 2.9, 4, 5, 7, 9, and 12 GHz.

Table 3: Bias and frequency for IMD measurements

f_1 (GHz)	f_2 (GHz)	Vgs(V)	Vds(V)	Bias type
1.1	1.101	0	5	100% I_{dss}
1.1	1.101	-0.9	5	50% I_{dss}
1.1	1.101	-1.7	5	10% I_{dss}

Source power was swept from -20 to +18 dBm in 1 dBm steps and output power was measured at fundamental and IMD3 frequencies using spectrum analyzer. Power losses (cables etc.) were calibrated up to the probe tips.

After obtaining measured data, all models were simulated using the ADS harmonic balance feature to obtain output power at fundamental and IMD3 frequencies. At each frequency and bias point, an average error in dBm between measured and simulated data was calculated over the range of input available powers.

5. MODEL COMPARISON

The various models are compared by plotting the output power P_{out} vs. frequency for 100% I_{dss}, 50% I_{dss} and 10% I_{dss}. Figures 3 and 4 show the plots for the errors between the measured P_{out} at fundamental and IMD3 and the ones obtained from simulations. From the plots we observe that the errors tend to "stabilize" above 5 GHz i.e. there is not much change in errors from one frequency point to another, whereas there are significant changes below 5 GHz. We also observe a sharp increase in errors at 4 GHz. The source of this is under investigation; it could be due to some resonance set up by, e.g., an isolator whose cut-off is at 4 GHz.

From Figure 3 one can qualitatively conclude that Statz model provides the best overall fit, i.e. across the frequency and bias range, for P_{out} (or gain) at fundamental frequency. In the lower frequency range differences between models are less pronounced. At the 10% I_{dss} bias, Curtice Cubic and Angelov's model had significantly larger errors at frequencies larger than 4 GHz.

Figure 4 shows somewhat surprising level of error for IMD3 results. For 100% and 50% I_{dss} bias points, results for different models are reasonably close to each other, but Curtice cubic performs the best. Near cut-off, i.e. at 10% I_{dss}, Advanced Materka and Statz show the best results.

6. CONCLUSIONS

Previous work done on the comparison of the non-linear MESFET models was extended by including the Angelov's model and extending the measurements and model predictions of the IMD to 1-12 GHz range. In terms of DC fit, all models had similar errors, except near cut-off, where Curtice cubic and Statz model showed significantly better results. C-V curves were best fitted by Angelov's model. When it comes to IMD, at this time it is difficult to establish a single best model for use across the frequency range and bias points, since some models are more accurate but only in a relatively limited range. One model that did show a reasonably uniform accuracy was Statz model. Interestingly, despite having the best fit to C-V curves and very good DC performance, Angelov's model didn't show any remarkable improvement over other models in terms of IMD performance. This may change once we evaluate the performance for the linear bias point, where a better C-V fit at lower Vds voltage may become important.

Ultimately, we want to find the dominant non-linear mechanism for different models. This would shine some light on how to improve the models and potentially also help us understand how to improve the device performance. This study is an initial step toward that goal. Future work will also address reasons for 4 GHz spikes in error, difficulty in matching the linear region of I-V curves, as well as adding more models, such as TOM3.

7. REFERENCES

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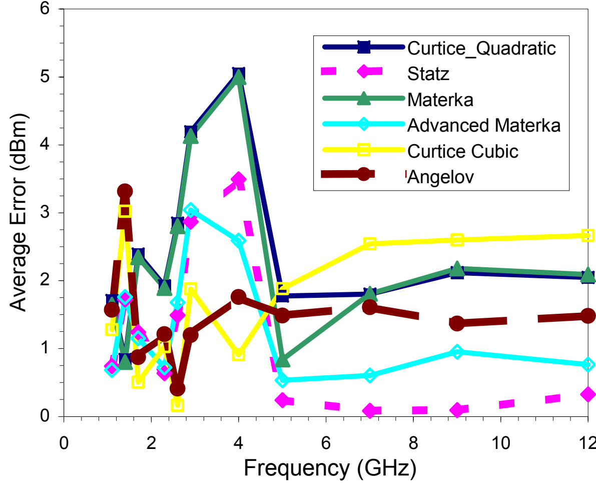
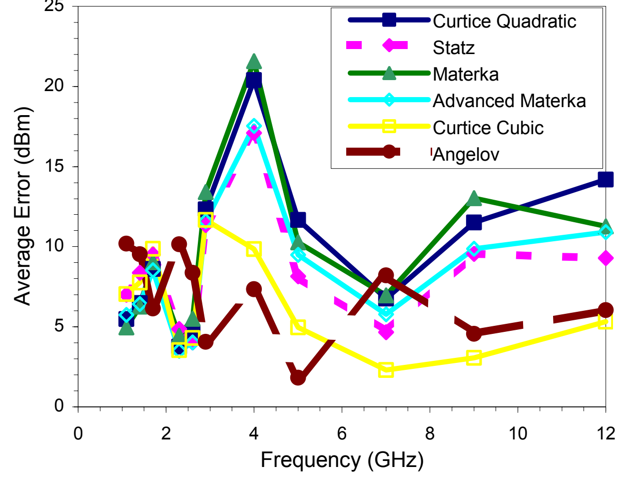

a) 100% Idss, fundamental
Average Error (dBm)
Frequency (GHz)
Curtice_Quadratic
Statz
Materka
Advanced Materka
Curtice Cubic
Angelov


a) 100% Idss, IMD3
Average Error (dBm)
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Curtice Quadratic
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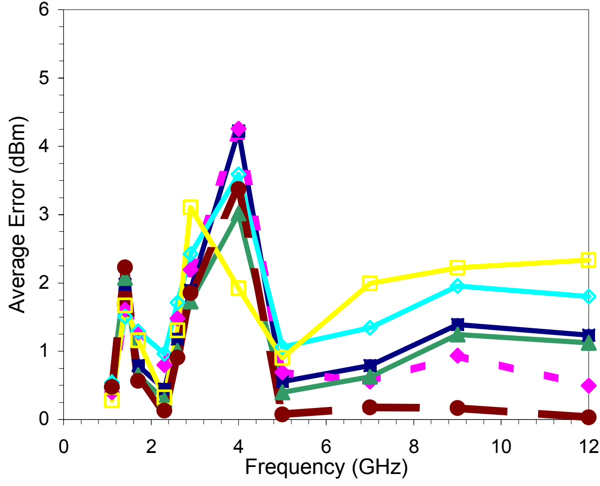
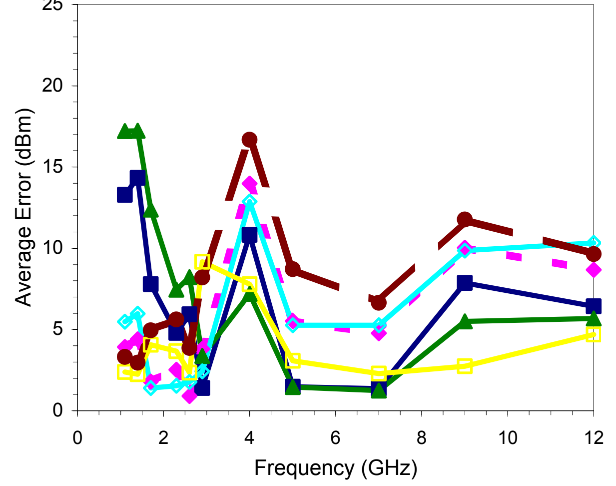
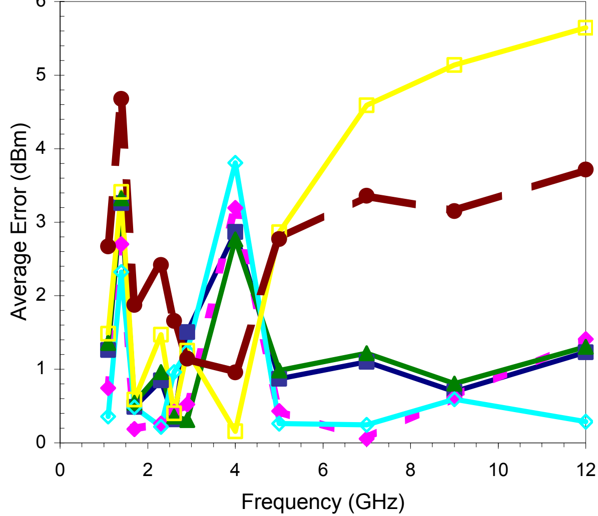
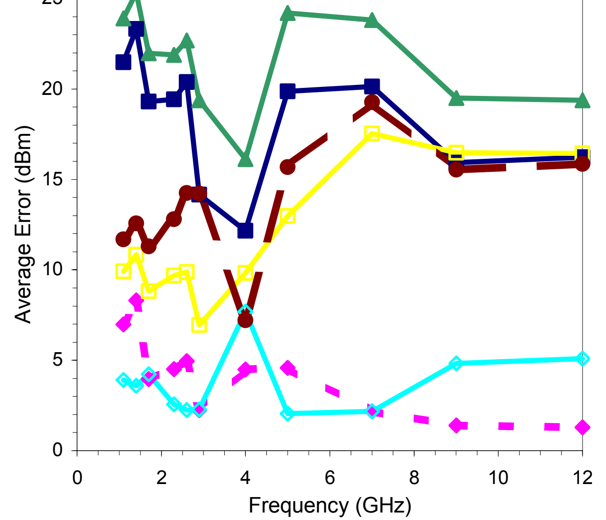

b) 50% Idss, fundamental
Average Error (dBm)
Frequency (GHz)


b) 50% Idss, IMD3
Average Error (dBm)
Frequency (GHz)


c) 10% Idss, fundamental
Average Error (dBm)
Frequency (GHz)


c) 10% Idss, IMD3
Average Error (dBm)
Frequency (GHz)