DSP BASED SYSTEM FOR SYNCHRONOUS GENERATOR EXCITATION CONTROLL

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Abstract—32-bit 150 MIPS fixed point DSP TMS320F2812 is used to develop control system for excitation control of synchronous generator. System is based on eZdsp board with DSP and development tool VisSim and Code Composer. At the moment in this system is implemented classical control structure and neural network based control structure.

Keywords: Modelling, Neural networks, DSP, Generator excitation systems

1 INTRODUCTION

In order to improve control characteristic of existing control system new system based on Texas Instruments DSP TMS320F2812 is developed. Beside classical regulation structure in this system is implemented neural network in order to improve regulation characteristic. TMS320F2812 is placed on eZdsp board. Two development tools for programming and simulation are used VisSim and Code Composer. VisSim is graphical based programming tool and it is used for simulation and code generation. Code Composer is integrated development environment tool from Texas instruments that have C compiler and it is used to complete DSP project (implementation of control structure and peripheral control of DSP).
At the moment two control structures are developed and implemented in order to perform control of excitation control of synchronous generator, classical with PI control algorithm and adaptive neuron.
Excitation of synchronous generator is connected to AC/DC converter controlled by DSP. For program download, on-line changing parameters and observation eZdsp board is connected thru parallel cable with PC.

2 THE TMS320F2812 DSP

The TMS320F2812 DSP is a member of the TMS320C28x DSP generation. It is 32-bit 150 MIPS DSP with on-chip flash memory and on chip analog peripherals (Fig. 1.) and its architecture is optimized for C. The IQ math library allow user to start code development in floating point space [1].

TMS320F2812 has following peripherals integrated on chip:

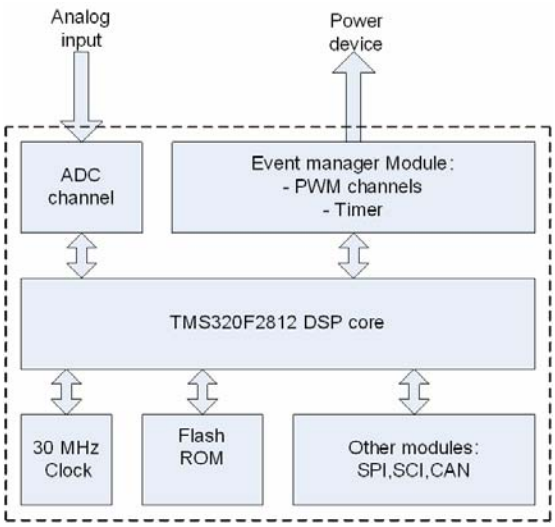

Fig. 1. TMS320F2812 block diagram

- **Peripheral Interrupt expansion (PIE) block**: multiplexes interrupt sources into smaller set of interrupt inputs. PIE block can support up to 96 peripheral interrupts which are in group of eight is fed in one of 12 CPU interrupt lines.
- **eCAN** : enhanced version of the CAN peripheral
- **Multichannel Buffered serial Port (McBSP):** is used to connect to telephone lines or for modem application.

- **Serial port Interface (SPI**): high-speed synchronous serial I/O port that allows a serial bit stream of programmed length to be shifted in or out of device.
- **Serial Communications Interface (SCI) :** two wire asynchronous serial port (UART)
- **Analog to Digital converter (Fig 2.):** have 12-bit resolution with single conversion time of 200 ns and

pipelined conversion time of 60 ns. It has 16 channels that can be configured as two independent 8 channels to service event managers A and B or they can be cascaded to form a 16 channel module. In ADC module there is only one converter. Analog input voltage is from 0 to 3V, and has dual simultaneous sampling or sequential sampling modes [2].

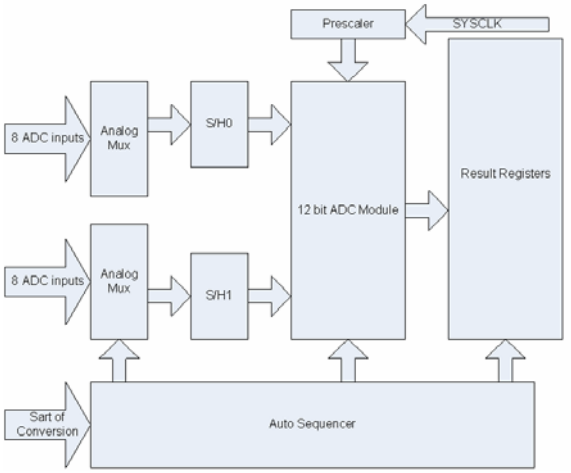

Fig.2. On chip 12 bit analog to digital converter

- **Event Manager (EV)**: include general purpose timers, full compare PWM units, capture units and quadrate-encoder pulse circuits.
- **General purpose Timers (GP)**: there are two GP timers for EVA and EVB. The compare register associated with each GP timer can be used for compare function and PWM waveform generation, GP timers can provide time base for other event manager sub modules.
- **Full compare units:** there are three full compare units on each event manager. Compare units use GP timer as the time base and generate six outputs for compare and PWM waveform generation.
- **Programmable Dead bend Generator: pr**oduce two outputs for with or without dead band zone for each compare unit output signal [3].

3 EZDSP F2812 BOARD

The eZsp board (Fig.3. and 4.) is stand alone card for development and run of the software for TMS320F2812 processor. Communication with PC has been established thru custom parallel port/JTAG interface device. The device has direct access to integrated JTAG interface. On chip memory is consisted of 128k x 16 Flash, two blocks of 4k x 16 SARAM, 8k x 16 SARAM, two blocks of 1k x16 SARAM and of chip memory is 64k x16 SARAM[4].

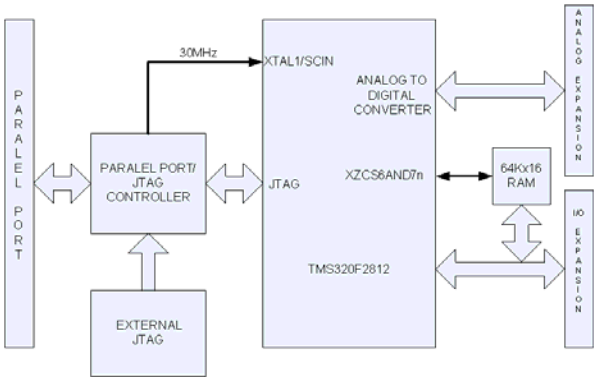

Fig.3. eZDSP F2812 board Bloc diagram

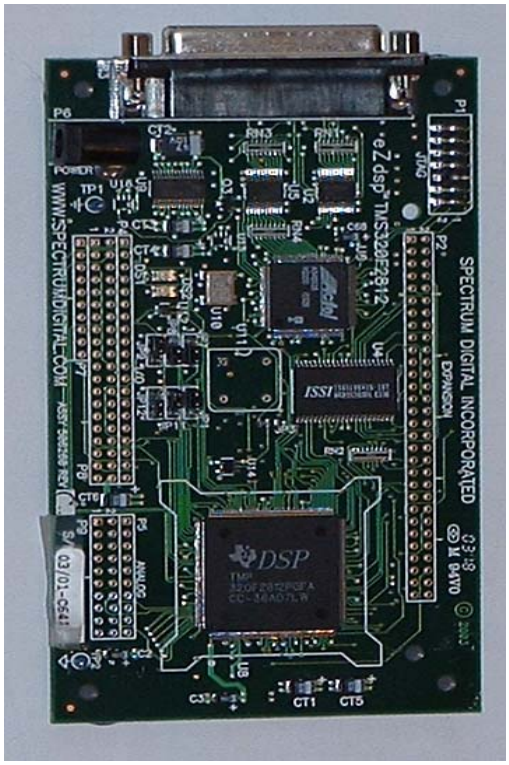

Fig.4. eZdsp Board

In order to supply eZdsp board with signals from synchronous generator we needed to develop interface board to adjust signal level

4 SOFTWARE DEVELOPMENT TOOL

Two types of software were used for programming TMS320F2812 Code Composer and VisSim.

Code Composer

Designed for the Texas Instruments TMS320Cx family of processors. It is development environment that have following capabilities and components: Integrated development environment (editor, debugger, project manager…), C compiler assembly optimizer and linker, instruction set simulator, real time foundation software, real time data exchange between host and target, real time analysis and data visualization (Fig.5).

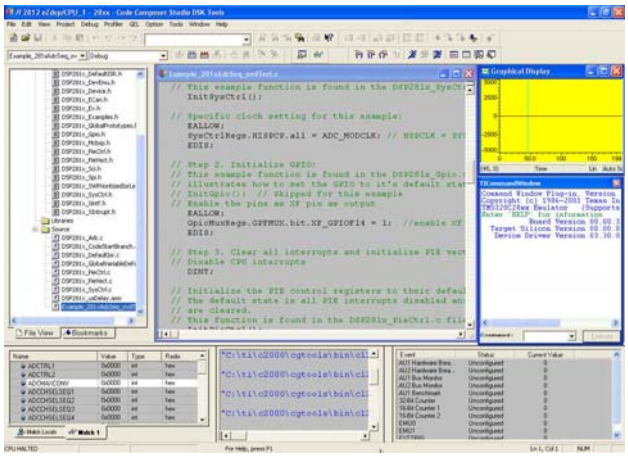

Fig.5. Main window in Code Composer

Steps taken in the DSP software development (Fig 6.) is following: writing C code on the host PC, compiling and optimizing and assembling and linking [5].

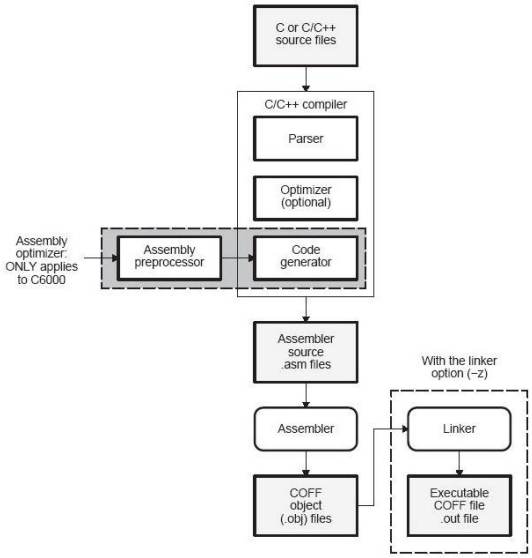

Fig.6. Code development flow

VisSim

VisSim embedded controls developer is software for fast code development for Texas instruments C2000 DSPs (Fig.7.). It is graphical programming with predefined blocks and target specific blocks. When the model of the plant is completed it is simulated in VisSim to verify algorithm behavior, results are viewed in graphical plots [6].

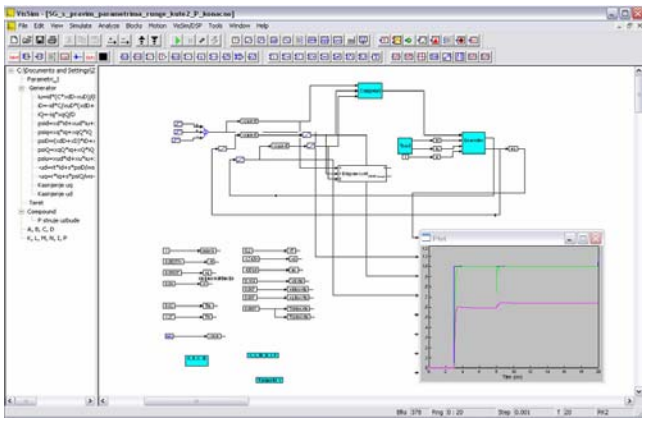

Fig.7. VisSim software main window

Also supports DSP in the loop simulation, where controller can be run on the DSP and inputs can take from VisSim and write outputs to VisSim. VisSim can generate fixed point C code from diagram drown in VisSim and has Code Composer plug-In. That means that algorithm developed in VisSim can easily be integrated in other user developed code.

5 CONTROL STRUCTURE

Two control structures are developed cascade regulation structure with PI algorithm and neural network based control.

Control structure with PI algorithm is consisted of voltage controller and excitation current controller (Fig 8.). Voltage controller is PI type and current controller is P type. Outputs of both controllers are limited [7].

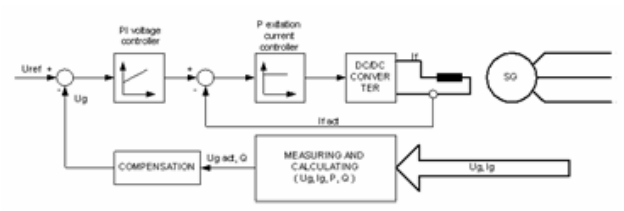

Fig.8. PI based control structure

Second control structure developed is based on adaptive neuron (Fig.9.)[7][8].

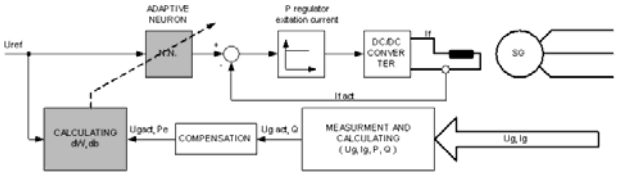

Fig.9. Adaptive neuron based control structure

6 NEURON

This adaptive neuron (fig.10.) is consisted of two parts. The one is single neuron which is regulator and in regulation structure is placed on the position of voltage regulator, and second part is modified error function that calculates weights and bias for neuron.
Neuron is consisted of one weight, one bias and activation function that is hard limit type.

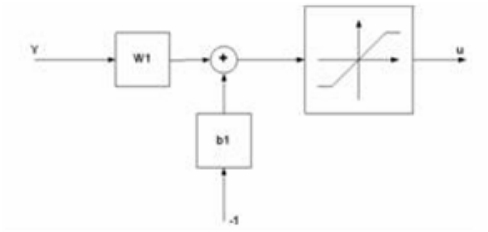

Fig.10. Adaptive neuron

Output of the neuron can be calculated on the following way:

$$u = y \cdot W_1 - b_1 \tag{1}$$

Changes of weight and bias based on the BP algorithm can be calculated on the following way:

$$\Delta W_1 = \eta \cdot error \cdot y \tag{2}$$

$$\Delta b_1 = -\eta \cdot error \tag{3}$$

Variable *error* represents modified error function. That variable can be calculated on the following way:

$$error = \left[\left(V_{ref} - V_t \right) - k_v \left(\frac{dV_t}{dt} \right) \right] \tag{4}$$

Meaning of symbols in upper equation is: V_{rej}- voltage reference, V_t - terminal voltage, k_v - constant.
Equation (4) represents error calculation for voltage control. Input in adaptive neuron is voltage reference and output is reference for current controller.

7 DSP IN THE LOOP

Simulation setup has made in VisSim development environment. Some exceptions during this simulation have been made. Synchronous generator is not connected on the network. Only one load is connected to the generator Fig.11. Frequency (speed) of generator is constant and we assumed that there is no nonlinearity in generator. Synchronous generator and load has been modeled and represented with block Fig.13. Control structure with PI controllers has been made according to Fig.8. Program segment consisted of voltage controller with PI characteristic and excitation current controller based on the P algorithm is shown on Fig.12. Data exchange between PC and eZdsp board is made thru parallel port JTAG emulator link. Model of synchronous generator and the load is placed in VisSim simulation program. Automatic C code generation has performed and part of the program with PI controllers (presented on fig.12.) is downloaded in TMS320F2812. In this case simulation step time and program execution time in DSP is synchronized and was 0.01 s.

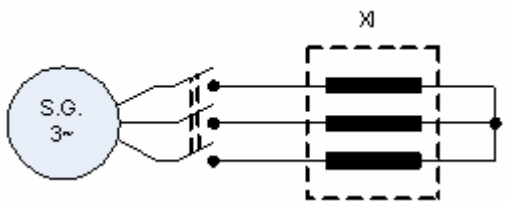

Fig.11. Generator and load connection

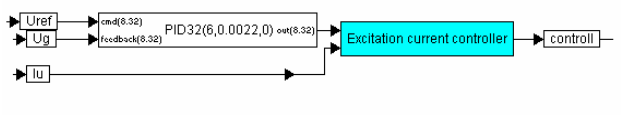

Fig.12. Cascade control structure in VisSim

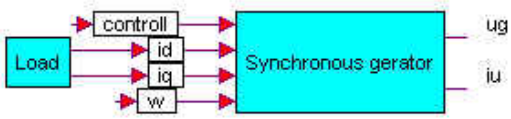

Fig.13 Synchronous generator and load

DSP in the loop simulation with TMS320F2812 linked thru JTAG emulator with VisSim has been done in real time for step voltage reference of 5 % and 10 % of the nominal voltage and it is shown on Fig.14 and 15. DSP used in this simulation is fixed point, according to that all program parts that will be executed in DSP must be written with fixed point blocks. Also all signals sends from VisSim to DSP and received from DSP must be in scaled integer format.

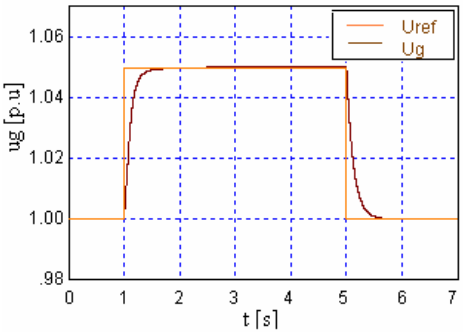

Fig.14. Response of terminal voltage for 5% reference step (PI voltage controller)

Adaptive neuron as mentioned before is placed on the position of voltage regulator and provides reference signal for excitation controller Fig.16.

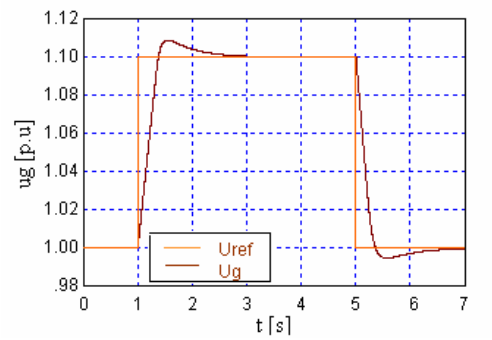

Fig 15 Response of terminal voltage for 10% reference step (PI voltage controller)

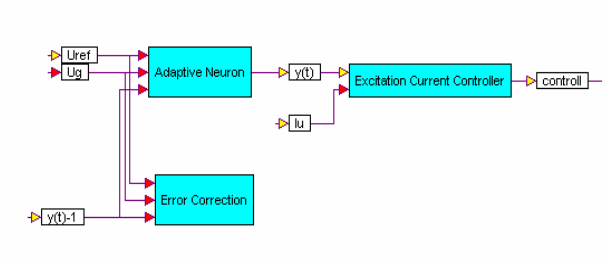

Fig 16 Implementation of adaptive neuron

Implemented control structure with adaptive neuron is tested for small step in reference voltage of 5 and 10 % of nominal reference. DSP in the loop simulation has been done in the some way as structure with PI controller mentioned before. Results are presented on the figures 17 and 18.

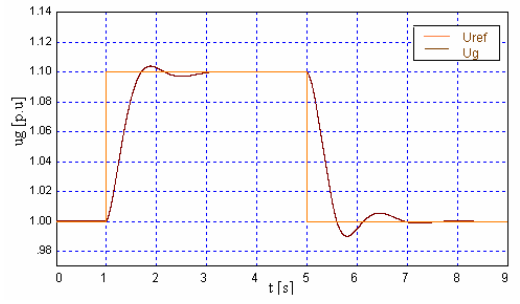

Fig 17 Response of terminal voltage for 10% reference step (adaptive neuron)

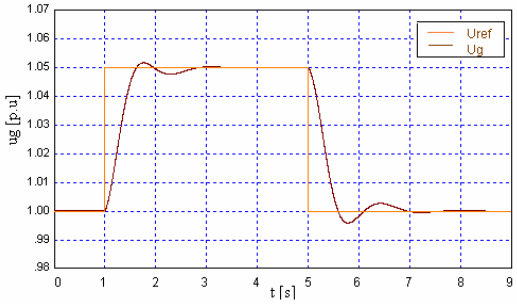

Fig 18 Response of terminal voltage for 5% reference step (adaptive neuron)

8 Conclusion

Excitation control system based on fixed point DSP TMS320F2812 and on Code Composer and development tools is very comfort for work. Development of algorithms in VisSim enables us at the same time to simulate algorithm and to test its behavior in DSP. Code Composer and Vissim Code Composer interface enables to include developed algorithm in some other algorithm or developed in Code Composer and provide us more space for control of DSP peripherals. TMS320F2812 is very fast and reliable fixed point DSP that operating on 150 MIPS. Some preliminary versions of this silicon have problems with analog to digital converter but in the newer versions they are solved. In the first versions of VisSim it was not possible to made adjustments in the work with analog to digital converter from VisSim window, but in new updates it is solved.

Experiments are done to determine response of existing algorithm in new hardware environment. Only few algorithms and their behavior are until now tested and simulated on this system in laboratory environment. In the future work more complex control algorithm will be implemented in this system.

Algorithm for adaptive neuron is simplified in compare with [7] and stabilizing effect for active power oscillations is not implemented.

Simulation setup parameters are:

Synchronous generator:
S=75kVA
U=400 V
Xd=0.8 p.u.
Xd`=0,35 p.u.
Xd”=0,15 p.u.
Xq”=0.15 p.u.
Td”=0.054 s

Load:
X=0.33 p.u.

9 References

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