Vertical Silicon-on-Nothing FET: Threshold Voltage Calculation Using Compact Capacitance Model

Boris Sviličić^a, Vladimir Jovanović^b, and Tomislav Suligoj^c

^a Faculty of Maritime Studies, University of Rijeka, Croatia, svilicic@pfri.hr, ^b ECTM-DIMES, Delft University of Technology, The Netherlands, ^c Faculty of Electrical Engineering and Computing, University of Zagreb, Croatia.

The silicon-on-nothing (SON) technology promises improved short-channel performance for ultra-scaled CMOS, without the added cost of the UTB SOI wafers [1]. The vertical fully-depleted SON concept (VFD SONFET) demonstrates the vertical SON structure, using the active transistor region grown on the sidewall of the Si/SiGe/Si stack with subsequent highly-selective SiGe removal [2]. As well as the improved SCE, the standard bulk region is eliminated in the VFD SONFET, making it a three-terminal device [Fig. 1 (a)] with well-controlled dimensions by the thickness of the grown layers [Fig. 1 (b)]. The absence of the transistor bulk is a unique property of the VFD SONFET, not present in either bulk or SOI CMOS, and the compact capacitance model is developed to describe the two-dimensional nature of this fully-depleted MOS structure. The calculation of the threshold voltage (V_{th}) using the compact model is presented in this paper.

The capacitance components of the VFD SONFET in the subthreshold region are shown in Fig. 2 [3]. Intrinsic capacities include the capacitance of the depleted silicon body $C_{Sl,d}$, gate oxide capacitance $C_{GOX}=k_{GOX}L_{eff}/t_{GOX}$, and buried oxide capacitance $C_{BOX}=2k_{BOX}\ln(1+L_{eff}/2d_{BOX})/\pi$. The buried oxide capacitance C_{BOX} of the VFD SONFET has specific, two-dimensional properties and its analytical relation is given with an approximation by perpendicular planes. For the effective channel lengths that are $t_{BOX} < L_{eff}/2$ analytical relation is $C_{BOX}=2k_{BOX}\ln(1+t_{BOX}/d_{BOX})/\pi$. Overlap, fringe and source/drain depletion capacitances are also included in Fig. 2, but do not have significant influence on the V_{th} . Equivalent capacitive circuit of the VFD SONFET in the subthreshold region is shown in Fig. 3, where V_{FB1} and Ψ_{s1} are the top-gate flat-band voltage and potential, and V_{FB2} and Ψ_{s2} are the back-gate flat-band voltage and potential.

The voltage-doping transformation (VDT) is used for the short-channel effects modeling [4]. According to the VDT, the effective channel doping is $N_A^* = N_A - k_{Si} 2V_{DS}^* / (qL_{eff}^2)$, where $V_{DS}^* = V_{DS} + 2(V_{bi} + \Psi_{s2} - \Psi_{s1}) \pm 2\sqrt{[(V_{bi} + \Psi_{s2} - \Psi_{s1})(V_{DS} + V_{bi} + \Psi_{s2} - \Psi_{s1})]}$. The silicon body capacitance with short channel effects (VDT) taken into account is $C_{Si,d}^* = qN_A^* t_{Si}L_{eff}/(\Psi_{s1} - \Psi_{s2})$, where $\Psi_{s2} = qN_A t_{Si}L_{eff}/(E_{BOX})$. The threshold voltage is determined from the strong inversion criterion $\Psi_{s1} = 2\Psi_b$, where $\Psi_b = V_T \ln(N_A/n_i)$. From the equivalent capacitive circuit, V_{ih} can be extracted as:

$$V_{th} = V_{G}|_{\Psi_{s1}=2\Psi_{b}} = V_{FB1} + 2\Psi_{b} \left(1 + \frac{2C_{Si,d} C_{BOX}}{C_{GOX} \left(C_{Si,d}^{*} + 2C_{BOX}\right)} \right) - V_{DS} \frac{C_{Si,d} C_{BOX}}{C_{GOX} \left(C_{Si,d}^{*} + 2C_{BOX}\right)} + 2V_{FB2} \frac{C_{Si,d} C_{BOX}}{C_{GOX} \left(C_{Si,d}^{*} + 2C_{BOX}\right)} \right)$$

where $V_{FB1} = V_{T} \ln(N_{G} N_{A} / n_{i}^{2})$ and $V_{FB2} = V_{T} \ln(N_{S-D} N_{A} / n_{i}^{2})$.

The calculated V_{th} values are compared to the results of the two-dimensional, drift-diffusion model simulations in MEDICI [5]. In Fig. 4, calculated and simulated threshold voltage values are plotted against L_{eff} for different t_{GOX} (a), channel concentrations (b), BOX dielectrics (c), and BOX thicknesses (d). Good agreement between our model and MEDICI data is achieved for L_{eff} down to 50 nm, with differences less than 5 mV (2 %). For L_{eff} below 50 nm, compact model loses accuracy due to rough approximation of the effective doping in the channel area N_A^* , which affects the calculated silicon body capacitance $C_{Si,d}^*$.

References

[1] M. Jurczak, T. Skotnicki, M. Paoli, B. Tormen, J. Martins, J. L. Regolini, D. Dutartre, P. Ribot, D. Lenoble, R. Pantel, S. Monfray, "Silicon-on-Nothing (SON) - an Innovative Process for Advanced CMOS", IEEE Trans. on Electron Devices, vol. 47, p. 2179, 2000.

[2] P. E. Thompson, G. Jernigan, J. Schulze, I. Eisele, T. Suligoj, "Vertical SiGe-based silicon-on-nothing (SON) technology for sub-30nm MOS devices", Materials Science in Semiconductor Processing 8, pp. 51–57, 2005.

[3] B. Sviličić, V. Jovanović, T. Suligoj, "Vertical Silicon-on-Nothing FET: Capacitance-Voltage Compact Modeling", MIPRO, 2007.

[4] T. Skotnicki, G. Merckel, T. Pedron, "The Voltage-Doping Transformation: A New Approach to the Modeling of MOSFET Short-Channel Effects", IEEE Trans. Electron Devices, vol. 9, no. 3, pp. 109-112, March 1988.

[5] Synopsys, Inc., Taurus Medici, Two-Dimensional Device Simulation Program, Version X-2005.10-0, 2005.





Fig. 2. Capacitive model of the

VFD SONFET in subthreshold region.

Fig. 1. (a) VFD SONFET structure cross-section, (b) VFD SONFET structure close-up.







ISDRS 2007 - http://www.ece.umd.edu/ISDRS