Modification of the Dickson charge pump clocking scheme for improved performance under capacitive load

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Abstract – This paper presents a modified Dickson charge pump that shows output voltage improvement under capacitive or very low current resistive loads. For capacitive load, depending on a number of pumping stages, the number of capacitors needed for achieving a certain output voltage decreases from 30% to 50%, with respect to the original Dickson charge pump. Modification takes place on the last pumping stage of a charge pump, and poses no limitation on the number of pumping stages to be used. A 4-stage modified Dickson charge pump was simulated and compared to the original Dickson charge pump.

I. ¹INTRODUCTION

Charge pumps are on-chip circuits used to generate DC voltage levels higher than voltage level available from the integrated circuit (IC) power supply. A charge pump consists of a number of pumping stages, where each pumping stage has a diode and one or more capacitors used to store charge and pass it to the next pumping stage. Stages are arranged in a chain, so that in an ideal case, the output voltage corresponds to a number of pumping stages. Every charge pump design has certain drawbacks due to voltage drop on diodes used in the design.

There are two most common usages of charge pumps. In the fisrt, one called a *direct usage*, voltage from the output capacitor directly supplies the electric circuit. Some circuits where this method is applied are high voltage generation for EEPROM circuits [1], FLASH memories [2] and implantable devices [3]. In the second or *indirect usage*, the electric circuit waits until voltage on the output capacitor reaches a certain voltage level, and then discharges the capacitor into a circuit allowing it to perform its function. This second method is more appropriate when the power available from the charge pump is insufficient for constant powering of the electric circuit [4], which can be found in RFID devices.

All these charge pump designs are based on the Dickson charge pump, and the output voltage they generate can be described by an expression similar to (1).

A 4-stage MOS Dickson charge pump circuit [5] is shown in Figure 1., the body of each MOSFET is connected to the ground (not shown in Figure 1.). The generated output voltage for Dickson charge pump with knumber of stages can be expressed as:

$$V_{out} = \sum_{i=1}^{k} (V_{DD} - V_{tni}) + (V_{DD} - V_{tnout})$$
(1)

, where V_{tni} is a threshold voltage of i^{th} and V_{tnout} of the output MOSFET and k is the number of indentical preoutput stages. Every stage added to a Dickson charge pump degrades efficiency because of the body effect of a diodeconnected MOSFET. In [6], [7], [8], [9], [10] modified versions of Dickson charge pumps are reported, where the output voltage drop and the pump efficiency are enhanced.

The proposed charge pump is also a modified MOS Dickson charge pump. We have decreased the number of capacitors needed for a defined output voltage by a slightly changed clocking scheme, resulting in:

$$V_{out} = 2 \cdot \sum_{i=1}^{k-1} (V_{DD} - V_{tni}) + (V_{DD} - V_{tnk})$$
(2)
$$-V_{tnout} - V_{tnS_1} - V_{tnS_2}$$

, where V_{tnS1} and V_{tnS2} correspond to switches M5 and M6 in Figure 3., respectively. Obviously, for the same number of stages, this approach gives a higher output voltage (see Eq. 1).





Fig. 1. 4-stage MOS Dickson charge pump and clock waveforms.

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Fig. 3. 4-stage modified Dickson charge pump and clock waveforms.

II. MODIFIED DICKSON CHARGE PUMP

Basically, the charge pump we propose is a Dickson charge pump with the last stage modified. Figure 2. shows this charge pump modeled by diodes and switches.

Modification of the Dickson charge pump consists of two switches added between two last stages of the pump. Figure 2. shows this modification applied on the 4-stage Dickson pump, but there is no limitation on the number of stages. The clock signals *clkA* and *clkB* are the same as in the Dickson pump. The idea behind this modification is the following. When switch S1 opens and S2 closes, it connects capacitors C3 nd C4 in series and in that way the output voltage reaches a value that is significantly higher than in the ordinary Dickson charge pump.



Fig. 2. 4-stage modified Dickson charge pump modeled with diodes and switches.

A full scheme of this 4-stage design and corresponding waveforms is showns in Figure 3.

The design consists of 5 diode-connected MOSFETs, M1 to M4 and Mout, and capacitors C1 to C4 and Cout. They form a classical Dickson charge pump. Additional MOSFETs M5 to M8, make the charge pump modification we propose. Also, the body of each MOSFET is connected to the ground, which is not shown in Figure 3., due to better clarity. MOSFETs M5 and M6 are switches S1 and S2, respectively. In order to ensure that switches can be completely turned on and off M7 and M8 are added. MOSFET M7 is a high resistance diode with switch M8 connected to the ground. While *clkA* is "high", switches M5 and M8 are on, and the ground voltage level is brought to the gate of switch M6. In this way, the M5 is turned on, and M6 is off. During that period capacitors are charging as in the Dickson charge pump. While clkA is "low", switches M5 and M8 are off, and the voltage level from capacitor C3 is through high resistance diode M7 brought to the gate of switch M6. In this way, the M5 is turned off, and M6 is on.

Now, capacitors C3 and C4 are serially connected and the voltage level transferred to the output capacitor is the sum of voltages from C3 and C4 (see Eq. 2). Simulation of the charge pump is done with Multisim 20001® software, using $0.35\mu m$ n-well CMOS level 49 SPICE models [11].

For exclusively capacitive load (no parallel resistive load to the output capacitor), comparison between output voltages of the Dickson charge pump and the modified Dickson charge pump we propose, for a differnt number of pumping stages, is given in Figure 4. The difference of output voltages increases with the number of used stages. This means that the modified Dickson charge pump is more appropriate for deveces where the number of stages is greater than 6, and the output voltage is 10 or more time higher than the supply voltage.



Fig. 4. Output voltage comparison for Modified Dickson and Dickson charge pump for a different number of pumping stages, V_{DD} =3.5V.

Output characteristics

Since the design is based on the Dickson charge pump, output characteristics of the proposed charge pump are compared with the Dickson charge pump. The tested charge pumps are both 4-stage pumps with 10 pF, 100 pF, and 1 nF capacitors, and the clock frequency is set to 1 MHz. V_{DD} voltage is set to 3.5 V. Results of comparison are shown in Figure 5., Figure 6., and Figure 7. The output currents are given both in linear and in logarithmic scale, so that low current section of output characteristics can be seen.





Fig. 5. Output voltages of Modified Dickson and Dickson charge pump under different output currents, linear and logarithmic scale, C=10pF, V_{DD} =3.5V.



Fig. 6. Output voltages of Modified Dickson and Dickson charge pump under different output currents, linear and logarithmic scale, C=100pF, V_{DD}=3.5V.



Fig. 7. Output voltages of Modified Dickson and Dickson charge pump under different output currents, linear and logarithmic scale, C=1nF, V_{DD}=3.5V.

The performance of the modified pump can be observed with the respect to output currents. For capacitive load, the proposed charge pump shows great improvement and corresponds to values shown in Figure 4. For resistive load, the modified charge pump shows improvement for lower currents, but output voltage deteriorates for higher currents in respect to a Dickson charge pump.

As it can be seen from the results of the comparison, the output current value at which the output voltage starts to deteriorate and proposed pump efficiency drops beyond the efficiency of the Dickson charge pump, is directly related to the size of the pumping capacitors.

But also, at that same output current value, the Dickson charge pump has 30% drop in output voltage with respect to output voltage when the charge pump is under high resistive load. With that in mind, the comparison results are showing that the proposed charge pump has improved efficiency and output voltage for the low current region, where the charge pumps are commonly used.

IV. CONCLUSION

A modified Dickson charge pump has been presented. It shows a great improvement in driving capacitive loads. As capacitors occupy most of the chip area, the fact that almost half of charge pump stages in an ordinary Dickson charge pump can now be removed offers a great chip area saving. Since the proposed charge pump under higher resistive load has improved output characteristics with respect to the Dickson charge pump, it can also be used in low current circuits that are directly powered from the charge pump. But, the best results of a modified Dickson charge pump can be expected in circuits that have capacitive load, or circuits that are indirectly powered. In those circuits the benefits of the proposed charge pump can come to the full extend.

REFERENCES

- J. S. Witters, G. Groeseneken, and H. E. Maes, "Analysis and modeling of on-chip high-voltage generator circuits for use in EEPROM circuits", *IEEE J. Solid-State Circuits*, vol. 24, p. 1372, 1989.
- [2] T. Tanzawa, and S. Atsumi, "Optimization of word-line booster circuits for low-voltage flash memories", *IEEE J. Solid-State Circuits*, vol. 34, p. 1091, 1999.
- [3] L. S. Y. Wong, S. Hossain, A. Ta, J. Edvinsson, D. H. Rivas, and H. Nääs, "A very low-power CMOS mixedsignal IC for implantable pacemaker applications", *IEEE J. Solid-State Circuits*, vol. 39, p. 2446, 2004.
- [4] F. Kocer, and M. P. Flynn, "A new transponder architecture with on-chip ADC for long-range telemetry applications", *IEEE J. Solid-State Circuits*, vol. 41, p. 1142, 2006.
- [5] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique", *IEEE J. Solid-State Circuits*, vol. 11, p. 374, 1976.
- [6] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Design of charge pump circuit with consideration of gate-oxide reliability in low-voltage CMOS processes", *IEEE J. Solid-State Circuits*, vol. 41, p. 1100, 2006.
- [7] J.-T. Wu, and K.-L. Chanag, "MOS charge pumps for lowvoltage operation", *IEEE J. Solid-State Circuits*, vol. 33, p. 592, 1998.
- [8] J. Shin, I.-J. Chung, Y. J. Park, and H. S. Min, "A new charge pump without degradation in threshold voltage due to body effect", *IEEE J. Solid-State Circuits*, vol. 35, p. 1227, 2000.
- [9] C. C. Wang, and J. C. Wu, "Efficiency improvement in charge pump circuits", *IEEE J. Solid-State Circuits*, vol. 33, p. 852, 1997.
- [10] C. Lauterbach, W. Weber, and D. Römer, "Charge sharing concept and new clocking scheme for power efficiency and electromagnetic emission improvement of boosted charge pumps", *IEEE J. Solid-State Circuits*, vol. 35, p. 719, 2000.
- [11] URL:
 - https://www.eecs.berkeley.edu/~boser/courses/software/spi ce/CMOS35/index.html