CPLD- and FPGA-Based Technology Applications in Embedded Systems Used in Transport and Industrial Control

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Abstract - In this paper are presented several possible applications in transport and industrial applications using complex-programmable logic device (CPLD)-based and field-programmable gate array (FPGA)-based technology. Problems dealing with overcoming gaps between existing local industry technology and new embedded systems technologies are discussed from a stand point of short and long term economic aspects. Several features are compared such as high speed, cost reduction and low-power consumption, design security, etc. New compromise solutions to some existing industrial applications are proposed in order to increase system efficiency and reliability.

***Keywords*— embedded systems, digital design, optimization.**

I. INTRODUCTION

There is a requirement for implementation of new technologies in existing old digital electronic industrial applications since old solutions are disused and too expensive to deal with. Implementation of complex programmable logic devices (CPLDs) and field programmable gate arrays (FPGAs) in industry and transportation are used in large-scale. The integration of glue logic and co-processing units into the low cost CPLDs is a very attractive proposition. Larger digital designs which have microprocessors and microcontrollers included, their corresponding interconnecting glue logic and co-processing units, may be replaced with a single FPGA chip. By the use of FPGA, digital design becomes simpler to test, implement, and reimplement. In this way, global system performance improves. At the same time board area, power operation and heat dissipation reduces.

This presentation deals with efficiency of digital design implemented into FPGA and CPLD devices using Very high speed integrated circuits Hardware Description Language (VHDL). Two different implementations are discussed. Expected performances of those designs are compared.

The rest of this article is organized as follows. Related works are proposed in section 2. Efficient digital design example is presented in section 3. Section 4 deals with possible future work, and conclusion is done in section 5.

II. RELATED WORKS

The integration of digital design into the FPGA, illustrated in Fig.1, has two basic approaches.

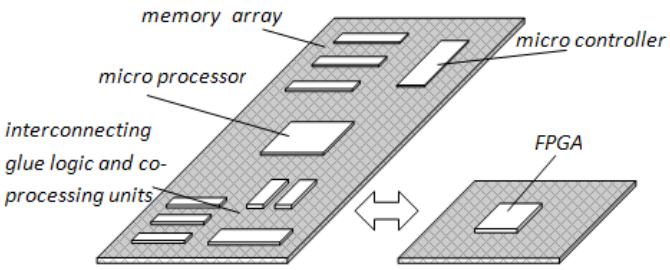

Figure 1. Advantages of FPGA in digital design.

It can be done either as a generic hardware/software co design or as a pure hardware design. Hardware/software co design approach allows digital system to act as generic reconfigurable device (RD). Real world hardware problems are solved with RDs via sequence of instructions, i.e. software, downloaded through interface between personal computer (PC) and FPGA. Pure hardware design represents single complex instruction predetermined to solve one real world hardware problem. Hardware/software co design is more generic and easier to implement and reimplement while pure hardware design is faster [2].

Digital systems with speed as its basic feature may be designed with SiGe FPGAs because they provide the highest operating frequency. Digital design which does not require GHz signal frequencies may be designed with standard low-cost CMOS based FPGAs. Hybrid digital design using both SiGe and CMOS based FPGA was done in [3] where data acquisition system (DAC) is proposed as high speed operation design with GHz signal bandwidth.

Heat emission reduces by replacing several chips with a single FPGA chip (see Fig.1.). Additional 33% of heat reduction is possible [7] when appropriate FPGA temperature-aware placement and routing algorithm is applied.

Implementation of FPGA technology is popular for multimedia applications where large amount of data are processed via parallel computation. Processing time in such systems is calculated by the sum $t = t_A + t_P$, where t_A is data acquisition time, and t_P is data processing time. References [1] and [5] are examples of multimedia applications using pictures taken from camera and processing unit on FPGA chip.

III. DIGITAL DESIGN EFFICIENCY

High operating frequency is main digital design feature. Digital design in general should be as much concurrent as possible, thus using CPLD and FPGA resources efficiently. Such digital design requires multiple processes, i.e. maximal parallelism possible. Besides high frequency, digital design may be optimized from standpoint of low-power dissipation, low-cost investment, board area [6], heat emission [7], and code simplicity so designer can easily understand it while doing redesign [2].

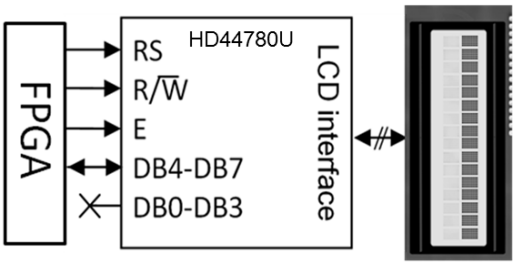

Figure 2. Interface scheme of HD44780U LCD controller display driver in 4-bit mode operation.

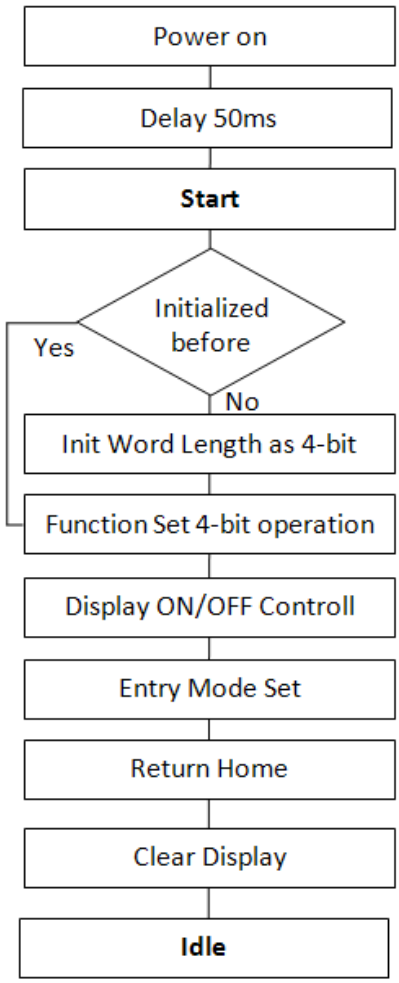

Figure 3. Flow chart of HD44780U LCD controller display driver initialization in 4-bit mode operation.

Fig. 3 illustrates HD44780U LCD controller display driver input/output pins for 4-bit mode operation [8]. For purpose of this work, LCD display driver in 4-bit mode operation is considered, while 8-bit mode is also possible. Proposed device controls LCD display functions. With use of FPGA it displays characters on LCD display.

In order to compare digital designs efficiency finite state machine (FSM) illustrated in Fig. 3 is implemented in two different ways.

Fig. 2 illustrates flowchart for HD44780U LCD controller display driver initialization in 4-bit mode operation [8]. When power is on, FSM is in start state and 50ms controller function is set to manufacturers default 8-bit mode operation. If controller was not initialized before, default 8-bit word length should be changed to 4-bit word length. Thus, in case when reset signal appears, initialization is not required. FSM states Function set, Display on/off, Entry mode set, Return home, Clear display, and Idle initializes proposed controller. States of FSM determines several input signal values, as it is illustrated in Fig. 3.

```
process(current_state, next_state)
begin
case current_state is
   when START =>              -- Start
      next_state <= WORD_LEN;
   when WORD_LEN =>           -- Init Word Length
      en <= '0';
      next_state <= WORD_LEN_A;
   when WORD_LEN_A =>
      en <= '0'; rs <= '0'; rw <= '0';
      next_state <= WORD_LEN_B;
   when WORD_LEN_B =>         -- Upper Bits
      data <= "0010"; rs <= '0'; rw <= '0'; en <= '1';
      next_state <= WORD_LEN_C;
   when WORD_LEN_C =>
      en<='0';                -- without Lower Bits
      next_state <= WORD_LEN_D;
   when WORD_LEN_D =>
      next_state <= FUNC_SET;
   when FUNC_SET =>           -- Function Set
      en <= '0';
      next_state <= FUNC_SET_A;
   when FUNC_SET_A =>         -- Upper Bits
      data<="0010"; rs<='0'; rw<='0'; en<='1';
      next_state <= FUNC_SET_B;
   when FUNC_SET_B =>
      en<='0';
      next_state <= FUNC_SET_C;
   when FUNC_SET_C =>         -- Lower Bits
      data<="0000"; rs<='0'; rw<='0'; en<='1';
      next_state <= FUNC_SET_D;
   when FUNC_SET_D =>
      next_state <= DISPLAY;
   ...
end process;
```

Figure 4. Example FSM1 with less optimization.

TABLE I. EXPECTED PERFORMANCES.

Parameter	FSM1	FSM2	Improvement
Frequency [MHz]	300.300	321.854	6.70%
Power consumption [W]	0.368	0.343	7.29%
LUT resources used [%]	0.285	0.472	- 65.6%

Part of VHDL code is illustrated in Fig. 4 and Fig. 5. FSM1 illustrated in Fig. 4 is less optimized than the FSM2 shown in Fig. 5. Synthesis report proposed in table 1 shows that the FSM2 has better performances than the FSM1. Operating frequency and power consumption for FSM2 is approximately 7% better when compared with the FSM1. Thus, FSM1 is more optimized then the FSM2. When assigning signal values, FSM1 has sequential sequence in difference with FSM2 which assigns all output signal values at the same time.

```
process(current_state, next_state, state_cnt)
begin
   case current_state is
   ...
   when START=>          -- Start
      next_state <= WORD_LEN;
   when WORD_LEN=> -- Init Word Length
      if state_cnt = "11" then  next_state <= FUNC_SET;
      else next_state <= WORD_LEN;
      end if;
   when FUNC_SET =>  -- Func Set
      if state_cnt = "11" then  next_state <= DISP_ON;
      else next_state <= FUNC_SET;
      end if;
   when DISP_ON =>      -- Display On/Off
   ...
end process;

process(reset, clkout, state_cnt, current_state, next_state)
begin
   if (reset = '1' or next_state = INIT) then  en <= '0';
   elsif rising_edge(clkout) then
      if ((state_cnt(0) = '0'  or next_state = INIT_2)
         and not(current_state = START)) then
            en <= '1';        -- set Enable Signal
      elsif (state_cnt(0) = '1' or next_state = INIT_3
         or next_state = INIT_1) then
            en <= '0';        -- reset Enable Signal
      end if;
   end if;
end process;
```

Figure 5. Example of FSM with more optimization.

However, number of slice LUTs is increased from 82 to 136 out of 28800. More available FPGA resources were spent due to design parallelization. Thus more resources are needed when more processes are used. In case of FSM2 there are processes for every input/output signal used. FSM2 has 9 processes, while FSM1 has two processes, one process for changing states, i.e. FSM, and one process for clock divider, i.e. prescaler.

IV. FUTURE WORK

An algorithm for ceramic tile surface inspection with machine vision [4] can be implemented by the use of FPGAs. Performances of machine vision ceramic tile visual quality inspection may be improved by replacing an existing sequential algorithm that runs on PC, with a systolic algorithm that runs on FPGA. An algorithm for classification of ceramic tiles can be decomposed into smaller tasks and pipelined. Basic idea is to apply low cost FPGA embedded system instead of a PC.

V. CONCLUSION

The use of CPLDs and FPGAs is more and more present in transport and industrial systems. In this paper optimization of applied digital design was proposed using VHDL. Synthesis reports show that speed and power-consumption performances are improved by approximately 7% (table 1) after appropriate optimization was done. Little down side of designs parallelization is that certain amount of LUT resources was increased by 65%. Experimental results confirm the importance of digital designs optimization.

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REFERENCES

[1] A. Amir, L. Zimet, A. Sangiovanni-Vincentelli, S. Kao, “An embedded system for an eye-detection sensor”, Elsevier Science Inc., Computer Vision and Image Understanding, Vol. 98 , No 1, pp. 104-123, 2005.

[2] P. P. Chu, RTL hardware design using VHDL, A Wiley-Interscience publication, ISBN-13: 978-0-471-72092-8, 2006.

[3] J.R Guo, C. You, K. Zhou, M. Chu, P.F. Curran, J. Diao, B. Goda, R.P. Kraft, J.F. McDonald, “A 10 GHz 4:1 MUX and 1:4 DEMUX implemented by a Gigahertz SiGe FPGA for fast ADC”, Integration, the VLSI Journal, Vol. 38, pp. 525-540, 2005.

[4] Ž. Hocenski, T. Keser, A. Baumgartner, “A Simple and Efficient Method for Ceramic Tile Surface Defects Detection”, Industrial Electronics, ISIE 2007. IEEE International Symposium on, ISBN: 978-1-4244-0755-2, pp. 1606-1611, 2007.

[5] A. Kumar, S. Sarkar, R.P. Agarwal, „A novel algorithm and FPGA based adaptable architecture for correcting sensor non-uniformities in infrared system“, Microprocessors & Microsystems, Elsevier Science Publishers B. V. Amsterdam, Vol. 31, Issue 6, pp. 402-407, 2007.

[6] K. Parnell, N. Mehta, Programmable Logic Design Quick Start Hand Book, Xilinx inc., 2002.

[7] K. Siozios, D. Soudris, A Novel Methodology for Temperature-Aware Placement and Routing of FPGAs, IEEE Computer Society Washington, Proceedings of the IEEE Computer Society Annual Symposium on VLSI, pp. 55-60, ISBN:0-7695-2896-1, 2007.

[8] Datasheets for HITACHI HD44780U controller, http://web.mit.edu/6.115/www/datasheets/44780.pdf