Efficient and Reusable Offset Cancellation Method Implemented in CMOS Design

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Abstract – An efficient and reusable offset cancellation method is presented, applicable for all amplifier structures with input resistances. The offset is cancelled with the current injected into amplifier's split input resistances. To keep the compensation range equal over the all working conditions, the compensation current is generated using the resistor from the voltage reference, matched with the amplifier's resistors. The compensation current value is generated with the simple IDAC structure, controlled by SAR or even a simple counter, depending on the available compensation time. Such approach requires a simple circuitry and it is very easy to implement. The effect to compensated amplifier's noise and linearity is low and controllable, while the effect to the gain accuracy doesn't exist. Additional advantage of using current instead of voltage for compensation is in insensitivity to interferences. By using a simple circuit for offset cancellation range adjusting, the proposed method becomes reusable.

I. INTRODUCTION

For a resistive gain chain, especially with a large required gain, offset error is, by nature, an issue which should be solved for correct and acceptable overall functionality.

Depending on the requirements for the overall gain, as well as the remaining offset error at the output, offset cancellation points (loops) can be put on one or more places.

The main purpose of the offset cancellation is to cancel various offsets coming from input, from the modules inside the gain chain, etc. resulting in minimum remaining offset error at the output without affecting the signal dynamic across the gain stages.

II. PRINCLE OF OPERATION

Among several possibilities for offset cancellation implementation, the simple one was chosen and modified. Offset cancellation is realized by differential current injection into split stage's input resistors. The compensation current is generated from a bandgap voltage reference and determined by an appropriate resistor value. To keep the offset cancellation ranges invariable over all working conditions, the stage's resistors and the resistor in the voltage to current converter block should be matched. Although such approach needs a very simple circuitry easily implemented, it is accurate, robust, and also insensitive to interferences. In addition, with such an implementation, the influence to the gain stage's linearity and noise is very small and quite acceptable.

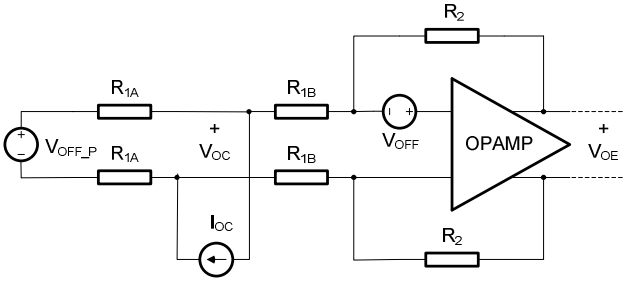

Fig. 1. Offset errors and cancellation

Figure 1. shows the simplified offset cancellation scheme. The stage's offset error is emulated by an independent voltage source V_{OFF} and the remaining offset error from the previous stages by V_{OFF_P}. The offset error at the output caused by V_{OFF} and V_{OFF_P}, which should be compensated, is represented by V_{OE}. The needed compensation current is represented by I_{OC} and the resulting offset compensation voltage by V_{OC}.

Such approach has additional advantages: easy compensation polarity change; meaning sign implementation which actually increases compensation resolution for one bit; and secondly easy adjustment. As the zero value is defined, it is enough to take care of the necessary compensation range only.

Additional important advantage of the presented approach is that the ratio $R_{1B}/(R_{1A}+R_{1B})$ defines the compensation current value and, assuming the real current source, affects the linearity of the signal path.

It is easy to calculate current needed to compensate the known offset error at the output V_{OE}:

$$V_{OC} = 2 \cdot \frac{R_{1A} \cdot R_{1B}}{R_{1A} + R_{1B}} \cdot I_{OC} \tag{1}$$

$$V_{OE} = V_{OC} \cdot \frac{R_2}{R_{1B}} \tag{2}$$

$$V_{OE} = 2 \cdot \frac{R_{1A}}{R_1} \cdot I_{OC} \cdot R_2 \tag{3}$$

With the known offset error at the output, the appropriate compensation current is:

$$I_{OC} = \frac{V_{OE} \cdot R_1}{2 \cdot R_{1A} \cdot R_2} \tag{4}$$

In case of a small stage's offset error, the offset cancellation loop can be implement on a cascade of gain stages. With $gain_{CR}$ as the gain of following cascade stages (cascade without the first stage), the necessary compensation current is:

$$I_{OC} = \frac{V_{OE} \cdot R_1}{2 \cdot R_{1A} \cdot R_2 \cdot gain_{CR}} \tag{5}$$

The implemented offset cancellation loop is shown in more detail by Figure 2. The offset cancellation current is generated with IDAC (current mode digital to analog converter) controlled by SAR (Successive Approximation Register) logic, but a simple counter is quite acceptable, in many cases. IDAC is followed by a simple current range block (simple current mirror) and a simple differential current driver with polarity control. Such approach allows us to use practically the same loop for different application points after correct adjustment of the current range block, for fully differential and for single ended outputs, as well.

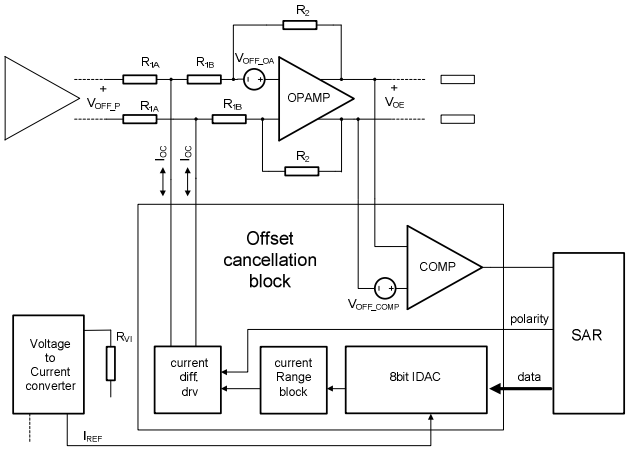

Fig. 2. Offset cancellation loop block scheme

With known offset errors for the used OPAMP and comparator (simulated using Monte Carlo analysis with process and mismatch model variation and maximum available number of samples), we are able to calculate the real offset error and the required offset cancellation range.

For calculation, the worst case is assumed:

- offset errors are used as positive (polarities of offset errors are defined in such a way that the resulting offset error at the stages' outputs are maximal and positive)
- the maximal gain is used in case of variable stage's gain

At the beginning, since:

$$I_{OC} \approx \frac{V_{BG}}{R_{VI}} \tag{6}$$

where V_{BG} is the bandgap (or any reference voltage), than:

$$\frac{V_{OE}}{V_{BG}} \approx \frac{2 \cdot R_{1A} \cdot R_2}{R_{VI} \cdot R_1} \tag{7}$$

With resistor matching and by keeping resistance ratios constant, stable compensation range over all working conditions is achieved.

The offset error at the stage output is:

$$V_{OE} = \left(V_{OF\_P} \cdot gain + V_{OFF\_OA} \cdot (1 + gain)\right) \tag{8}$$

where

$$gain = \frac{R_2}{R_{1A} + R_{1B}} \tag{9}$$

For the offset cancellation range and the remaining offset error calculation, the maximum gain value is important.

The calculated value defines the output offset cancellation range. For the real system, this value should be slightly enlarged, multiplied with some k_{OC} (1.05-1.1), because of temperature dependency, uncalculated mismatch (squared ratio), gain errors etc.

After offset cancellation, the remaining offset error at the gain chain output is:

$$V_{OE\_REM} = \frac{k_{OC} \cdot \max(V_{OE})}{2^n - 1} + V_{OFF\_COMP} \tag{10}$$

where n is the IDAC's resolution, in bits and $k_{OC} \cdot \max(V_{OE})$ is the cancellation range at the output..

The simulation results show that calculations were quite correct.

III. IMPLEMENTATION

A. General Information

The presented offset cancellation loop and gain stage were part of front-end, organized as a cascade of stages with a very high overall gain. The circuit was designed, simulated and verified in the 350 nm technology across the process corners and the temperature range. The design of circuit can be processed in any available mixed–signal technology with necessary re-calculations and optimizations due to the specific characteristics of the technology.

To save space and to keep a clear picture, only some of the schematics will be shown. The top level schematic is similar to the offset cancellation block scheme (Figure 2.). The used R-2R MOS IDAC architecture is well known and the corresponding schematic will be avoided also.

In the design, all resistors have the same unity resistance to achieve matching and R_{1A} and R_{1B} are equal.

B. Voltage to Current Converter

The voltage to current converter (Figure 3.) is simple and well known circuit, with the bandgap voltage as the

reference. Voltage-to-current converter uses a resistor with the same unity resistance as the resistors in affected gain stages. Resistances should be matched in the layout to avoid the changes of the compensation ranges over the process variations and working conditions. In case of restrictive area requirements, in case when multiple offset cancellation loops are required, the voltage-to-current converter can be implemented as common, shared between different offset cancellation loops.

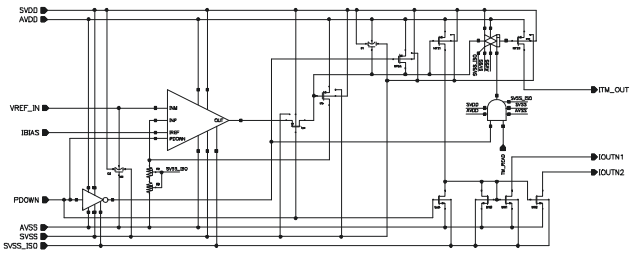

Fig. 3. Voltage to current converter

C. Comparator

Regarding to requirements, for different offset cancellation loops, different comparators should be used. The used comparator was optimized for fully differential input signals. As the remaining offset error always depends on the used comparator's offset error, regardless to compensation resolution and range, the comparators were also optimized regarding to their own offset error.

D. IDAC

For the described offset cancellation loop a simple, but optimized, 8 bit R-2R MOS IDAC was chosen. The IDAC is controlled by a SAR regarding to the limited time available for the compensation. The SAR was implemented with the polarity control (sign, equivalent to additional bit).

The compensation range is 8 bits with the sign (polarity, equivalent to 9 bits resolution).

E. Current Range Blocks

The current range block (Figure 4.) is a simple current mirror, used for a simple offset cancellation range adjustment. Such an approach allows us to reuse the same offset cancellation loop, even to share the same voltage to the current converter for different loops.

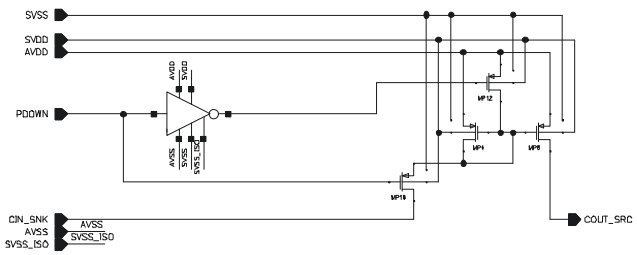

Fig. 4. Current range block

F. Differential Current Driver

Differential current driver (Figure 5.) is a single-ended to fully-differential current converter, having the possibility to change the output current polarity. Although directly connected to the signal path, because of the differential, symmetrical structure connected to the differential signal path, the impact to the signal being processed is minimal. Leakage does not present a problem due to the fact that the differential signal is affected in both planes acting as a common signal.

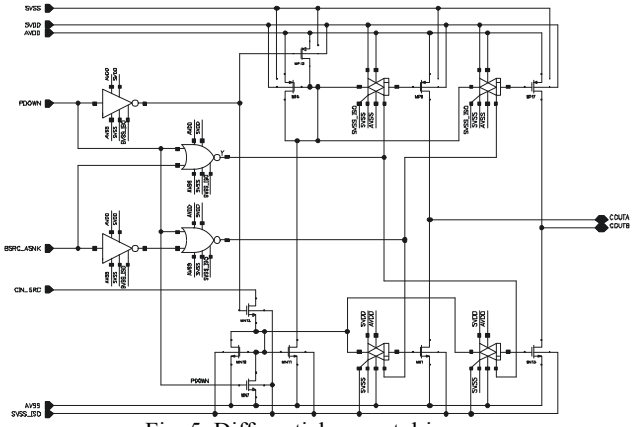

Fig. 5. Differential current driver

IV. VERIFICATION

Offset cancellation in real gain chain was simulated over all working conditions, using ideal voltage sources for particular offset error emulations.

Working conditions are all process corners; temperature range: -40 +125ºC; power supply voltage: 3.2 – 3.6V and bias currents (operational amplifiers): 93 – 107% of the nominal values.

Polarities of offset error voltage sources were chosen to give the worst possible errors over gain chain stages.

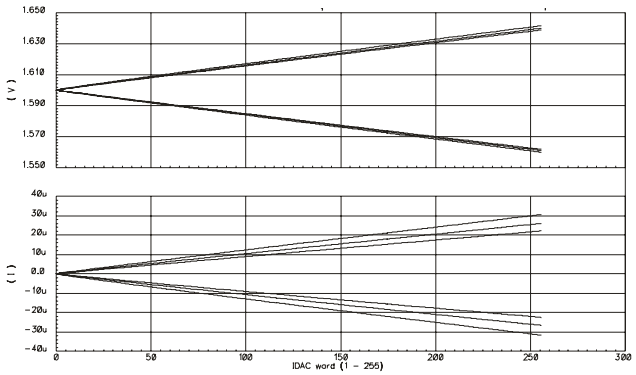

Fig. 6. Offset cancellation voltage and current ranges, the worst case

Figure 6. shows the offset cancellation voltage (V_{OC}) and current (I_{OC}) over all IDAC's input values. The nominal and the worst cases (min and max) over process corners and working conditions are shown. Maximal values actually represent compensation ranges.

As expected, regarding to technological resistor's value variation, the current range is also changed. With required resistors matching, the voltage range is acceptably stable. As the offset error is practically constant over all working conditions for any particular corner, the achieved range stability fit our needs.

TABLE I
Offset cancellation voltage changes, all cases

OC voltage range, all cases		
Min. [-%]	Nominal [mV]	Max. [+%]
-2.39	78.8924	3.46

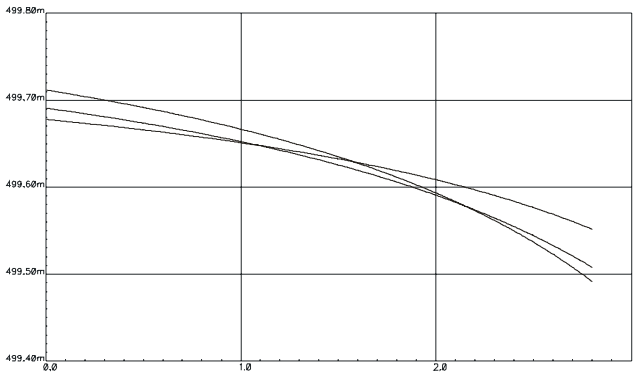

Fig. 7. Influence to the gain stage linearity error

Figure 7. shows the signal path linearity error caused by the offset cancellation loop, for full signal swing, with its nominal and the worst cases over all process corners and working conditions.

TABLE II
Linearity error over all working conditions

Linearity error, all cases	
Nominal [%]	Max. [%]
± 0.018	± 0.022

Figure 8. shows the output voltage (V_{OE}) during the offset cancellation with the IDAC controlled by the SAR logic, over all process corners and working conditions. Offset errors were chosen to cause maximal negative offset errors at the output.

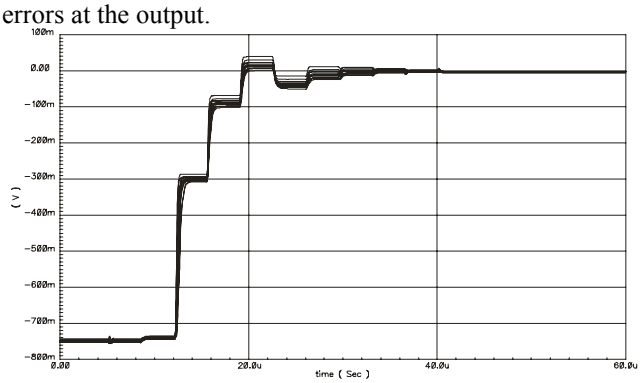

Fig. 8. The output voltage VOE, during offset cancellation, all cases, negative offset error

Figure 9. shows the output voltage (V_{OE}) during the offset cancellation with the IDAC controlled by the SAR logic, over all process corners and working conditions. Offset errors were chosen to cause maximal positive offset errors at the output.

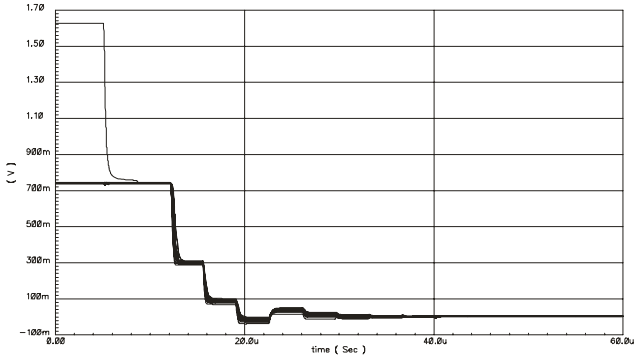

Fig. 9. The output voltage VOE, during offset cancellation, all cases, positive offset error

Figures 10. and 11. show the output voltage (V_{OE}) for the case with the gain stage which performs fully-differential to single-ended conversion, both cases regarding to the offset error polarity.

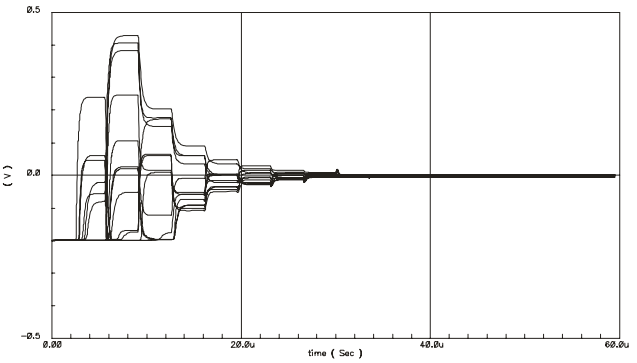

Fig. 10. The output voltage VOE, single-ended output, during offset cancellation, all cases, negative offset error

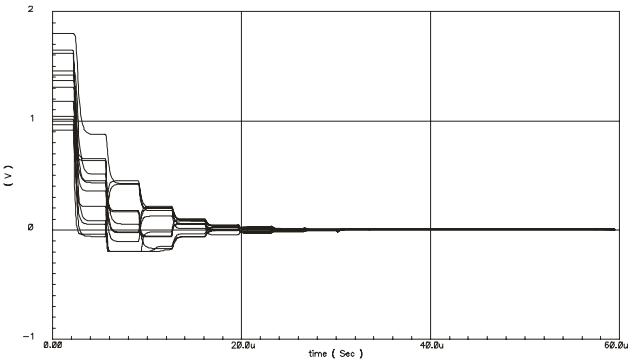

Fig. 11. The output voltage VOE, single-ended output, during offset cancellation, all cases, positive offset error

V. CONCLUSION

An efficient and reusable offset cancellation method is presented. It is applicable for all amplifier structures with input resistances.

Reuse of the proposed offset cancellation method is simple. The compensation current range should be calculated and the current range block (simple current mirror) should be adjusted after a correct splitting of stage's input resistors (regarding to acceptable effect to the linearity error). It is enough for almost all applications in resistive gain stages with differential inputs.

In the case of smaller offset errors, or in the case of a single-ended input architecture, some simplifications of the presented circuits are possible.

REFERENCES

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