The Role of Post-Layout Verification in Microprocessor Design

Dubravko Marković, Dejan Ljuština, Radenko Cvijetić[1], Danko Ivošević, Oliver Rohtek, Mario Rotim
Systemcom d.o.o, Zagreb Design Center
Maksimirska 120, 10000 Zagreb, Croatia
Phone: (+385) 1 2335 880 Fax: (+385) 1 2339 590
E-mail: dubravko.markovic@systemcom.hr; dejan.ljustina@systemcom.hr; radenko.cvijetic@intel.com; danko.ivosevic@systemcom.hr; oliver.rohtek@systemcom.hr; mario.rotim@systemcom.hr

Nanometer technology and high chip frequency place high demand on the EDA (Electronic Design Automation) tools to reliably and efficiently find design problems in post-layout verification process. The only way to tackle designs with over billion transistors on a single chip is to use the knowledge and skill of highly experienced engineers in constant development and improvement of layout verification tools and methodologies.

The purpose of this article is to present methodology and new challenges in layout verification and reliability checks of todays microprocessor layout designs.

I. INTRODUCTION

In a constant race with smaller and smaller chips it is of great importance to develop reliable and efficient post-layout verification methodology based on the usage of state-of-the-art software tools tailored to the specific needs of the verification process. This can only be achieved by combining knowledge, experience through generations of chip design, and off-course, constructive team work efforts.

In order to verify geometrical properties, electrical properties, functionality and reliability of a huge layout designs every tool used in verification flow has to efficiently deal with the hierarchical concepts that are used to divide initial layout into smaller segments suitable for processing and also appropriate on the certain stage of analysis.

The flow from the drawn chip layout to the verified analysis outputs can be divided into the following areas by their functionalities:

- LVS (Layout Versus Schematic) Layout verification with the main purpose to check electrical connectivity of the drawn objects and to verify schematic equivalence.
- DRC (Design Rule Check) Geometric Verification should ensure that the layout conforms to the manufacturing and yield rules.
- Parasitic extraction provides the source data for the analysis of the electrical properties of drawn geometry. This demanding task involves rather complex and sophisticated extraction algorithms and data structures to generate accurate chip interconnect parasitic networks out of connectivity geometric database obtained by preliminary LVS and DRC processing.
- Reduction of extracted large parasitic networks is the enabling step for the analysis where we are interested not in exact geometrical circuit properties but in electrical characteristics like timing analysis and more.
- Interconnect verification step should ensure that our design will actually work. It should point engineers to problematic layout where there is potential for failures due to electromigration (EM) effects, IR drop, self-heat effects, antenna effects, RC skew conditions.

Although we mentioned these five areas as a separate fields they should all be well integrated into complete verification methodology supported by the adequate software tools.

II. LVS LAYOUT VERIFICATION

Main goal of LVS layout verification is to verify that the chip layout implements the circuits from the schematics, and to generate the layout transistor netlist. LVS is the main connectivity engine and platform for the parasitic extraction and the interconnect analysis tools. LVS also plays important role in the chip layout methodology support (net naming, chip verification). Inputs to LVS are flat or hierarchical layout geometry, schematic netlist, and the control file specifying the connectivity relationship between layers in the layout. Data outputs are the layout transistor netlist, and various error files as shown on Fig. 1. Main components of LVS are Layout extractor and Netlist compare.

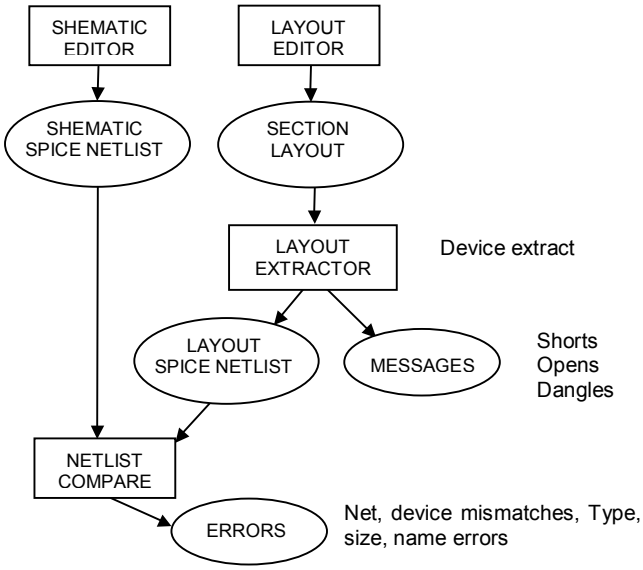

Fig.1. LVS flow.

[1] Mr. Cvijetić is currently with Intel Corporation, Hudson, Massachusetts.

A. Layout Extraction

Layout extractor determines layout connectivity, detects devices in layout, performs net naming and device netlisting, finds layout problems like shorts, opens and dangles (nets without device connections). Algorithms should be optimized to detect flat and hierarchical touches and overlaps between interacting geometry. Spatial information and width/length of polygon segments are not critical here. Layout connectivity is established by performing flat and hierarchical hookup between touching and overlapping polygons. The connectivity rules are described in the input technology file. Hierarchical pins are created at the point of hierarchical geometry interactions. Any existing pins in the layout are verified for correct names and connectivity.

Typical Layout extractor tool flow consists of:

- Reading polygons and breaking them into trapezoids.
- Walking through structures, recursively processing each placement.
- Processing flat geometry for structure to make devices, connecting touching trapezoids on the same layer and connecting overlapping metal, vias, and text.
- Hierarchically hooking up layers, text, vias.
- Following connectivity links to generate net names.
- Flattening names for open and dangle detection.
- Writing transistor netlist.

B. Netlist Compare

Netlist compare tool performs comparison of the flat or hierarchical schematic and layout graphs formed by the transistors and their connectivity. Additional operations include: device and stack merging (when wide devices and stacks are implemented as multiple fingers), and layout net and device name back-annotation (with the names from the schematics). Netlist compare also supports top level checks in a partitioned chip verification methodology.

Typical Netlist Compare tool flow consists of:

- Reading schematic and layout netlists
- Merging parallel devices and stacks
- Comparing netlists:
  - initially matching nets by name
  - initially matching devices by type
  - iterating between nets and devices using recent matches to determine new matching net or device pairs (graph coloring)
  - comparing hierarchical connectivity
- Comparison completes when either all nets and devices have been uniquely paired or no further matching occurs
- Write requested reports: matching devices, matching nets, errors

Mismatches between schematic and layout hierarchy result in explosions of the hierarchical levels. Consequences could be the net naming problems and also performance degradation.

C. LVS challenges

The challenges on the LVS tools include the following:

- Verification of large caches.
- Global net extraction and stitching.
- Chip LVS with growing database size.
- Metal routing architecture for easy verification.
- Avoiding cell overlaps for performance.
- Analog device recognition.
- Floating and connected transistor bodies in SOI.
- Die to package verification of bumps and wirebond pads.
- Output formats (ensuring compatibility with downstream tools).

III. DRC GEOMETRIC VERIFICATION

Main goal of DRC is to ensure that the layout conforms to the manufacturing and yield rules. Secondary goal is to allow layout migration and shrinks, and engineering checks. It is also used for layout productivity: contacts, wells, implants and dummy metal synthesis. Input to DRC is the geometry from the layout creation tools, and the manufacturing requirements in form of layout rules. Outputs are an error file (with DRC tick marks), and the layout geometry (if used in a layout productivity mode).

DRC checks typically consist of Standard and Project-specific rules. Basic checks verify the spacing, width, and enclosure of various layout objects. Algorithms are optimized to detect flat and hierarchical touches, overlaps, widths, lengths, and spacing. Connectivity information is important in specialized checks like the same net spacing or productivity scripts like automatic via generation.

Non-traditional use of DRC includes the following layout productivity applications:

- Automatic contacting and via generation.
- Power/ground grid and plate generation.
- Implant and well synthesis.
- Density checks and metal fill generation.
- Layout migration.
- Chip partitioning verification: clean belts, top checks.

Special DRCs are geometric checks used to supplement electrical engineering analysis tools:

- Diffusion and poly jumpers.
- Latchup (well plug to P device resistance).
- Bonus metal.
- ESD checks.

DRC challenges

Full chip DRC is becoming a challenge due to growth of chip database sizes. Runsets could be split into layer based checks and executed as multiprocessed jobs for improved throughput. RAM cells usually push the limit of layout rules. Important DRC property is the ability to recognize and tolerate DRC tickmark waiver layers to reduce unnecessary error reporting. Metal routing discipline and architecture are important for good DRC performance. Splitting geometry across cell boundaries slows down DRC and causes performance and memory problems.

IV.PARASITIC EXTRACTION

Chip interconnect parasitics are starting to dominate the overall capacitance and are critical for accurate circuit analysis. The primary function of the extraction tool is to provide accurate information on interconnect parasitics. Data input for the extractor are the connectivity geometric database and technology parameter file containing the physical information of the chip design process. Some of the requirements that are crucial for development of a tool for distributed RC and inductance extraction and reduction are high accuracy, geometric sizing and scaling capabilility, interconnect modeling with 2D and 3D field solver and multiprocessing for improving performance. The output from the extraction process are capacitors, resistors and inductors written to a file like SPICE wirelist, SPEF wirelist or any other format. The next few chapters describe particular features of resistance, capacitance and inductance extraction process.

A. Resistance Extraction

Critical step for the resistance extraction is to fracture geometry into resistance segments following the flow of the current. Extractor first merges net layout geometry into polygons, and then re-fractures it into resistance segments. Fracture lines are perpendicular to the current flow and are created on layout discontinuities, and are treated as subnodes. Additional subnodes are formed at the contact and via sites and the placement of pins and ports in Fig.2. Resistors are created between the subnodes. Resulting resistance values are stored with segment geometric properties for all segments.

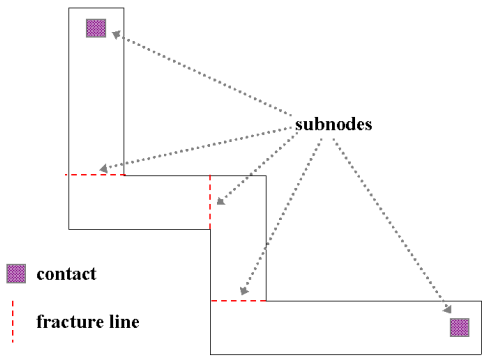

Fig. 2. Resistance geometric fracturing.

Some of the technology parameters relevant for the resistance extraction include temperature coefficients for material, sheet ρ and via resistances.

B. Capacitance Extraction

Primary geometric input to capacitance extractor are wide segments fractured into trapezoidal shapes. Extractor creates a search region from every real conductor segment edge and then searches for other interacting geometry. Region queries and layer geometry traverses could be implemented with quad tree data structures or scan lines. Thousands of simulations done by field solvers and curve fitting software are used to prepare capacitance model parameters that fit the analytical equations and are written into technology process file. Another approach would be to store simulated capacitance values directly in a large lookup table and not use analytical models at all. Particular geometry is decomposed into several basic profiles. These profiles could be: area, lateral, fringe to surface, edge to edge, and crossover. The area capacitance is modeled between the overlapping surfaces of conductors. Improvement to the algorithm could include shading effect of the conductors adjacent to the area profile. Lateral capacitance is formed by parallel edges of conductors on the same layer with shading layers above and below. The fringe to surface capacitance is formed between the edge of one conductor and the surface of another conductor above or below with varying surface width and presence of other shading conductors. Edge to edge capacitance is modeled between edges of conductors on adjacent layers with dependence on upper and lower spaces, inner distance, and the shading layers. Crossover model is a 3D model based on perpendicular conductors with dependence on upper and lower spaces, and the shading layers. Analytic formulae for calculating each profile can be seen in [1]. Fig.3. illustrates a common cross section with coupling capacitances represented in 2D.

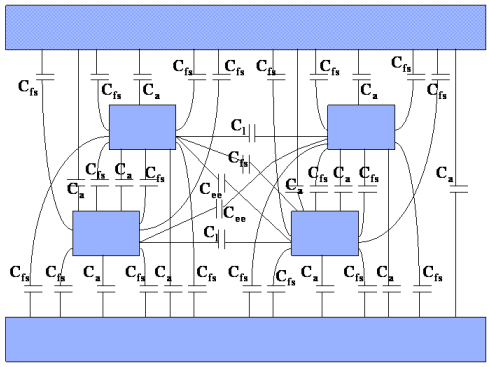

Fig. 3. Capacitance profiles.

The process of capacitance profiling starts with projecting a search region from a real edge of a conductor segment. Conductors with lateral coupling are processed first. Fringe capacitors are determined by intersecting search region to lower and upper layers. All capacitances are inserted into internal data structures. Distributed coupling capacitances are reported for every resistor.

C. Inductance Extraction

Inductance extraction is a very complex problem because of difficulty involved in determining the correct current return paths. Electromagnetic field spreads accross much larger distances and it is not as localized as the electrostatic field of the resistive effects.

First level of approximation in the inductance extraction is to assume that the current return paths are closed through the neighbouring power, ground and signal lines. Some of the solvers partition layout into sections bounded by power/ground lines. Fig.4. shows such localized interaction area with signal lines and its return current [2].

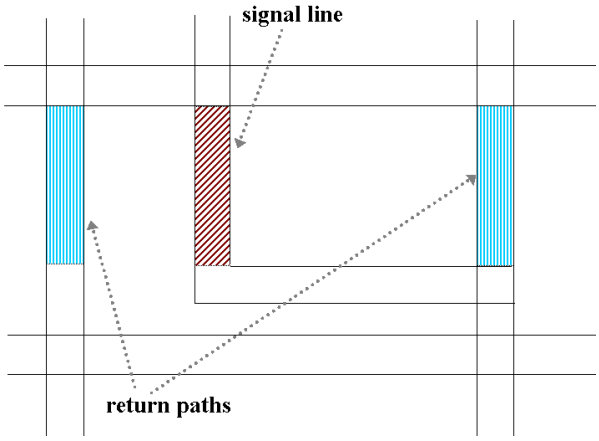

Fig. 4. Inductance interaction area.

The inductive effects are becoming much more important with the increase of the clock frequency and the introduction of low-resistance copper interconnect. Due to the lack of good inductance extraction and analysis tools significant effort is made to avoid these effects through power/ground shielding, repeater insertion and staggering, bit swizzling, etc.

V. REDUCTION ALGORITHM

Detailed analysis of interconnects is computationally expensive and not even possible for larger designs. The problem can be mitigated by using RLC reduction methods to reduce large and complex netlists. RLC reduction should not affect electrical behavior of the original netlist. RLC reduction is a compromise between two main parameters: required reduction ratio (up to 40- 60% or even 90%) and acceptable accuracy loss (few %). There are a number of methods and techniques for RLC (RC) reduction.

Traditional direction in the past decades are the model order reduction methods [8] focused on generating stable and passive macromodels. Such tools are based on Asymptotic Waveform Evaluation – AWE methods, PRIMA [9] and different moment matching methods. One interesting RC reduction method [5] is based on successive merging S-parameter sub-circuits which then produces reduced RC netlist for all S-parameter macromodels. The problem with this method is that a synthesis of the reduced RC netlist is not always possible and accurate enough, especially when applying this method to distributed RLC circuits.

An alternative approach in the RC and recently RLC reduction methods are the different node elimination methods (or more formal Gaussian elimination) like in the TICER (TIme Constant Equilibration Reduction) method [3]. TICER can be improved to handle RLC networks [6], [7]. In comparison to model order reduction this method is realizable and guaranties faster simulation and analysis. The basic principle of the node elimination method is to eliminate a node and all RLC elements connected to this node and then update impedance between all two neighborhood nodes. This is equivalent to star to delta (Y-Δ) transformation shown on the figure 5.

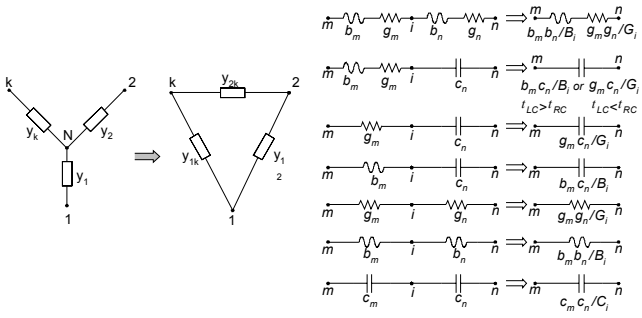

Fig. 5. Elimination of node *i* and rules for updating impedance between neighborhood nodes.

For the very large databases the performance of the original TICER algorithm can be improved with the additional node criteria to reduce node with smaller RLC elements first, and then to reduce nodes that have more incident reducible nodes. Furthermore the RLC reduction based on the node elimination method could be implemented as a parallel RLC reduction algorithm which can be executed in multiprocessing environment.

VI. RELIABILITY VERIFICATION

Due to ongoing chip miniaturization, thin-film metal interconnects are subject to extremely high current densities. This could cause electrical failure of conductors in relatively short time thus reducing circuit lifetime below statisticaly acceptable margin. Electromigration is phenomenon in which atoms in metal segments move when exposed to direct current, potentialy causing irreversible failures. If metal collects, hillocks could form and short out with neighboring lines, or cause cracks in the dielectric. If metal vacates, voids could form and cause a break in the metal interconnect. Bi-directional current flow will partialy repair metal segments by pushing atoms back into place.

Let us assume that we work on schematic shown on Fig. 6. The role of RV tool is to use extracted parasitic netlist obtained by parasitic extractor for the layout that realizes our schematic, then to compute currents for every metal segment of interest and apply adequate limits and verifications and report possible problems to users.

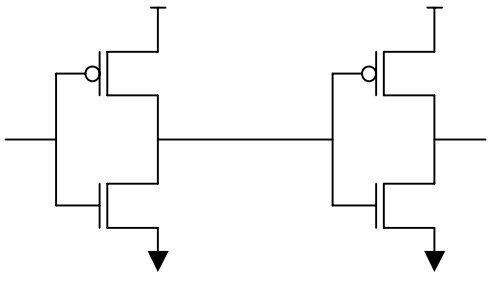

Fig. 6 Two inverter's example.

First step in RV tool flow is to read technology information in order to be able to apply appriopriate EM limits, extraction temperature, frequency, signal net activity factors obtained by logic simulators, etc. Then extracted distributed RC data is read together with geometry information and device netlist to form internal data structures and connectivity topology data. The tool

needs to identify the drivers (transistors connected to power/ground lines), receivers and parallel transistors whose gate signals switch simultaneously. The topology recognition step is required to identify the channel connected regions (CCR) formed by device channel connections and interconnects between power and ground lines.

In the analysis the transistors are treated as switches while capacitors are treated as current sources as shown on Fig. 7.

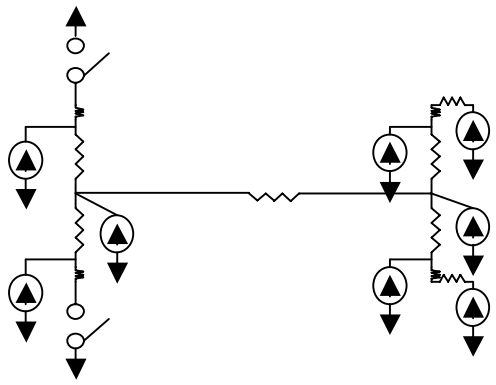

Fig.7.Non-CCR devices and caps treated as current sources.

At this stage all the information is available to form a system of linear equations, compute currents through resistor segments, determine current densities (J) and compare results against limits for the given technology process. I_{EFF} and I_{RMS} currents are used to check for EM violations for signal and power lines, and I_{PEAK} currents for voltage drop (IR) violations. There is a considearble requirement for the data capacity which can be solved by using a superposition method and the timing exclusivity information in order to improve the analysis perfomance.
Also for the power/ground network analysis, the tool divides the power grid into subnets between lower and upper via reference points along the layer stack and compute currents in a down to top fashion connecting upper vias to ground and using computed currents from the lower vias to excite subnets above stack.

Since fixing EM failures takes time, measures are taken in the early layout design stages to draw proper metal surround on vias that provide additional reservoir of atoms which helps reduce creation of voids. Not every metal segment running at $J > J_{limit}$ will fail during the chip lifetime, so statistical evaluation of the chip lifetime EM risk is used to assess the probability of failure. Current densities in the entire chip interconnect are analyzed by a statistical probability tool and chip EM risk is compared to the corporate standard.

Improperly designed power/ground interconnect can lead to voltage drop or ground bounce which could affect operation of transistors and chip failures. Voltage drop analysis of power/ground wiring is similar to power/ground electromigration analysis but it reports voltage drop amount instead of checking for current densities. Peak current with the worst case slopes is applied to find and report voltages at the transistors and identify devices which are subject to IR-drop. Circuit exclusivity hints are used to reduce the amount of false failures.

Additional very important task for RV tool is to check for overheated places on chip that could cause failure. Heat generated by the current flow can be calculated from the I_{RMS} current flowing through the interconnect segments. Most heat on chip flows laterally through metal, and vertically through vias. Furthermore, heat flux is received from touching segments and neighboring nets. This heat flux is likewise transferred to other segments and passed to the substrate. Heat network can be treated as a lossy electrical network to determine the temperature of endpoints, and the heat fluxes which are then used to adjust EM lifetime of segments.

Antenna effect is a layout-dependent gate dielectric damage mechanism where charge collected by conductors during manufacturing is transferred through interconnect and accumulates on transistor gates if they are electrically isolated. If enough charge is accumulated, the gate voltage rises to a value high enough for tunneling to occur. Gate electrode discharges through the gate dielectric causing immediate breakdown or latent damage. This damage can be prevented by providing shunting diodes to remove collected charge.

Antenna results need to be processed further to determine if there are any additional cumulative effects. Individual antenna ratios for poly, contact, vias, and all unsafe metals are added together and the cumulative ratio is compared against the technology parameter in order to find additional unsafe gates. Challenge in antenna processing is early analysis, and the analysis of the global nets.
Tool flow for the antenna effect is the following:

- Starting from the gates, identify unsafe conductor subnodes with no path to substrate.
- Find area of gate poly in unsafe paths.
- Find total area of poly and all metals in paths connected to transistor gate.
- Calculate area ratio of each layer in a path to the total area of gate poly.
- Check area ratios against technology rules and write error report.

Fix by placing diodes and connecting them near the failing poly gates.

The challenges in the reliability verification space are the following:

- Varying signal slope during I_{RMS} calculation to avoid pessimistic results near gate loads.
- Power/ground EM analysis is difficult due to inability to simulate realistic worst cases. This usually results in pessimistic overestimates with many false failures. Those must be examined by hand, which takes time and additional effort.
- Accurate 3D thermal analysis for EM application.

VII. CONCLUSION

We are all witnesses of the technological revolution in semiconductor industry that results in over billion transistors on a single CPU chip. This represents a huge challenge for the existing layout verification tools to be able to process the exhaustive set of data and to perform incremental verification with avoiding redundant steps as much as possible. On the other hand shortening the time to market forces chip designers to develop necessary support for early verification of incomplete layout in order to reduce the risks in the late development stage. General trends in microprocessor design forces engineers to put more effort on solving the inductance extraction and analysis, heat flow in chips with low-K dielectrics, mixed analysis of analog and digital circuits, accounting for process variations, accurate analysis in CBD methodology, and on many more challenges that nanotechnology brings along the way.

ACKNOWLEDGEMENTS

The authors would like to thank to Dr. Darko Gojanović, Mrs. Srebrenka Ursić and Mr. Damir Vuk for their great support.

REFERENCES

[1] N. Arora, K. Raol, R. Schumann, and L. Richardson, "Modeling and extraction of interconnect capacitances for multilayer VLSI circuits", IEEE Trans. Computer-Aided Design of Integrated Circuits, vol. 15, pp. 58-67, Jan. 1996.

[2] K. L. Shepard and Z. Tian, ``Return-limited inductance: A practical approach to on-chip inductance extraction," IEEE Transactions on CAD, pp 425-436, April, 2000.

[3] B.N. Sheehan, "TICER: Realizable Reduction of Extracted RC Circuits," Digest of Technical Papers, IEEE/ACM Proc. of ICCAD, pp. 200-203, 1999.

[4] A. J. van Genderen and N. P. van der Meijs, "Reduced RC Models for IC Interconnections with Coupling Capacitances", Proc. IEEE/DAC, pp. 132-136, 1992.

[5] H. Liao and W. W. Dia, "Partitioning and Reduction of RC Interconnect Networks Based on Scattering Parameter Macromodels", ICCAD 1995, pp. 704-09.

[6] Chirayu S. Amin, Masud H. Chowdhury, Yehea I. Ismail, "Realizable RLCK circuit crunching", Proc. IEEE/DAC, 2003.

[7] Zhanhai Qin, Chung-Kuan Cheng, "Realizable parasitic reduction using generalized Y-Δ transformation", roc. IEEE/DAC, 2003

[8] Lawrence T. Pillage, Ronald A. Rohrer, "Asymptotic Waveform Evaluation for Timing Analysis", IEEE Transactions On Computer-Aided Design, Vol. 9, No. 4, April 1990.

[9] A. Odabasioglu, M. Celik, L. T. Pileggi, "PRIMA: passive reduced-order interconnect macromodeling algorithm", Proc. IEEE/ACM CAD, 1997.