

A Low-Power Fully Differential 9-Bit C-2C Cyclic ADC

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Abstract— This paper describes a low-power fully differential cyclic ADC. It utilizes a 3-bit C-2C ladder to achieve 9-bit resolution. For the 9-bit resolution the 3-bit C-2C ladder occupies 64 times less area than a binary weighted capacitance array. The operational amplifier with the slew rate detection is used in order to increase the speed of the ADC. The simulated power consumption of the ADC is $33 \mu\text{W}@3.3 \text{ V}$ at the sampling rate of 10 kS/s. The DNL and INL are both less than 0.53 LSB. The spurious-free dynamic range (SFDR) is 63 dB and the signal-to-noise and distortion ratio (SNDR) is 54.2 dB. The equivalent number of bits (ENOB) is 8.7.

I. INTRODUCTION

Radio Frequency Identification (RFID) is a booming technology up to now mainly used as a replacement for barcodes. However, RFID technology is not limited only to barcodes; potential customers are requiring additional functionality such as various sensors [1]. For instance, in a case or pallet-level tagging the addition of sensors to RFID tags will allow monitoring of freshness of products, beverages and medical supplies in storehouses. Various environmental sensors will allow tracking of relevant parameters, e.g. temperature, light intensity, humidity, pH or gas composition. Such an RFID integrated with a sensor provides both information about the origin of the product and the conditions under which it has been transported, processed or stored.

The system consisting of an RFID enhanced with sensors imposes strict demands on power consumption in each block of the system since the available power is very limited. One solution is to use a battery supply (active tags), but the penalty is higher cost of RFID tags. The other option is energy harvesting from the light sources [2], vibration, thermal sources or electromagnetic waves (passive tags) [3] – [5]. Passive tags impose more challenging requirements since power is more limited than in active tags. First, e.g. electromagnetic energy must be collected from an antenna, stored in a capacitor and then delivered to the rest of the tag circuitry [3]. When the tag is active, the harvested energy stored in the capacitor, is decreasing as the capacitor discharges reducing the supply voltage. Due to their high power consumption bandgap references are not the best choice to obtain a stable and precise reference voltage for AD converters used in RFID tags. There are examples of very stable voltage references with respect to the temperature variation, but the reference voltage is not equally stable when the supply voltage changes [6]. The

influence of the power supply voltage variations can be substantially reduced by differential structures.

This paper presents a low-power fully differential 9-bit C-2C cyclic ADC. The ADC uses area-efficient 3-bit C-2C ladder to obtain a 9-bit resolution. The operation of the cyclic ADC is described in Section II. An operational amplifier, used in the cyclic ADC, is described in Section III. Section IV presents static and dynamic characteristics simulated with variations of the supply voltage. Section V brings conclusions.

II. SYSTEM OVERVIEW

The proposed fully differential cyclic ADC consists of a dynamic comparator and a reconfigurable circuit that can be used either as an amplifier or as a DA converter (Fig. 1). Both operations are needed to obtain a cyclic ADC. The mode selection (amplifier or DA converter) is obtained by the switches DAC_EN and AMP_EN . When one of these switches is on, associated path is connected to the input of the operational amplifier. In Fig. 1, $PH1$, $PH2$, SH_EN and D_i represent switches while V_{SGND} is the common mode voltage.

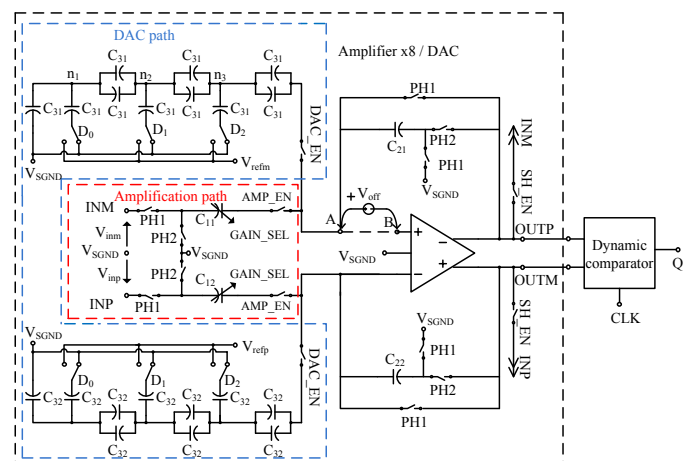


Figure 1. A fully differential 9-bit cyclic ADC.

A. DA converter

Binary weighted capacitor arrays and their variations are dominant networks in most ADC applications. From the layout point of view it is not the best solution because a very large

capacitor (MSB capacitor) must be matched with a very small capacitor (LSB capacitor). This leads to mismatch errors in capacitance causing lower resolution. Furthermore, these arrays consume very large area ($A = C_u 2^N$, where N is number of bits and C_u is the unit capacitance). The C-2C ladder is more appropriate solution for layout matching and area ($A = C_u(3N-1)$). Due to a large parasitic capacitance of the bottom plate, the resolution of the C-2C ladder is limited to only 4-6 bits without calibration [7].

The proposed AD converter uses a 3-bit C-2C ladder to achieve 9-bit resolution. For the 9-bit resolution, the 3-bit C-2C ladder in the proposed AD occupies 64 times less area than the conventional binary weighted arrays.

The operation of such a converter can be divided into 3 phases. Since the circuit is symmetric, only a half of the circuit will be analyzed.

B. First phase: Sampling and amplification

In the sampling phase (the switches $PH1$ are on while $PH2$ are off) the amplification path is selected (AMP_EN is on). The input signal and offset (modelled as V_{off} in Fig. 1) are sampled on the capacitor C_{11} . After the sampling phase the amplification phase is activated (the switches $PH1=off$, $PH2=on$). The sampled signal is amplified with gain 1 and stored on the capacitor C_{21} without the offset. The charge at the node A is:

$$Q_A^{SAMP} = C_{11}(V_{inm} - V_{off}) + V_{off}C_{21}, \quad (1)$$

$$Q_A^{AMPL} = -V_{off}C_{11} + (V_{off} - V_{OUTP})C_{21}. \quad (2)$$

After equalizing (1) and (2), the output voltage is

$$V_{OUTP}^{AMPL} = -C_{11}/C_{21}V_{inm}. \quad (3)$$

C. First phase: DAC operation

Once the amplification phase is over, the amplifier is configured into a DAC (DAC_EN is on). If the switch D_2 is on (i.e. the bottom plate of the capacitor C_{31} connected to V_{refm}), and D_1, D_0 are off, the output voltage is:

$$V_{OUTP}^{MSB} = -(C_{11}/C_{21})V_{inm} + (C_{31ek}/C_{21})\frac{V_{refm}}{2}. \quad (4)$$

The capacitance C_{31ek} is Thevenin's capacitance in the node n_3 (Fig. 1) and V_{refm} is the low reference voltage. If $C_{21} = C_{31ek}$, only a half of the reference voltage is amplified and added to the voltage stored in the amplification phase. If D_2 is off again, a half of V_{refm} will be subtracted from the voltage V_{OUTP}^{MSB} . This is equal to the contribution of the MSB in a conventional DAC. The contribution of the other bits is obtained from:

$$V^{DAC} = V_{refm} \left(\frac{1}{2}D_2 + \frac{1}{4}D_1 + \frac{1}{8}D_0 \right) - (C_{11}/C_{21})V_{inm}. \quad (5)$$

To calculate the contribution of other bits in Eq. (5) D_i must be set to one or zero depending on whether the corresponding switch is on or off.

D. Second phase

After the first phase is finished, the switches SH_EN are turned on and the second phase starts with the sampling of the residual voltage from the first phase at the input capacitors C_{11} and C_{12} (Fig. 1). The voltage from the output of the amplifier is sampled on the input capacitors. After some time the capacitors are charged to the residual voltage and sampling is finished. Using the same capacitors for sampling of the input voltages in the first phase and the residual voltage in the second phase is an area efficient approach. Also, capacitance matching is easier than using extra capacitors for the sampling of the residual voltage. In the next step the residual voltage is amplified 8 times to cover the maximum input voltage range. E.g. if the input voltage is equal to the reference voltage ($V_{in_max} = V_{ref}$) than the maximum residual voltage after the first phase, according to, (5), is

$$V^{RES} = V_{in_max} - 7/8V_{ref} = 1/8V_{ref} = 1/8V_{in_max}. \quad (6)$$

Digital signal $GAIN_SEL$ sets the gain to 8 by changing the value of the capacitors C_{11} and C_{12} .

In the second phase AD conversion starts after the amplification of the residual voltage.

E. Third phase

The residual voltage obtained in the second phase is again amplified in the third phase (Fig. 2) and finally 3 LSBs are obtained. The third phase concludes an ADC cycle.

Sampling, capacitors charging and amplification takes some time and defines the overall speed of the ADC. In order to minimize the number of the phases, 3 bits are obtained in each phase instead of resolving 1-bit per phase.

In the proposed ADC, low input voltages (voltages that are equivalent to 3 LSBs or less) are amplified 64 times (8 in the second phase and 8 in the third phase). E.g. if 1 LSB is equal to 4 mV in a conventional converter, then in the proposed approach 1 LSB is equivalent 256 mV, which means that the requirement on the offset voltage of the dynamic comparator (latch) in the second and third phase is relaxed. In the first phase the gain is 1 and an offset compensated preamplifier (e.g. [8]) can be used to relax offset of the latch. In the later phases the preamplifier can be switched off to save the power.

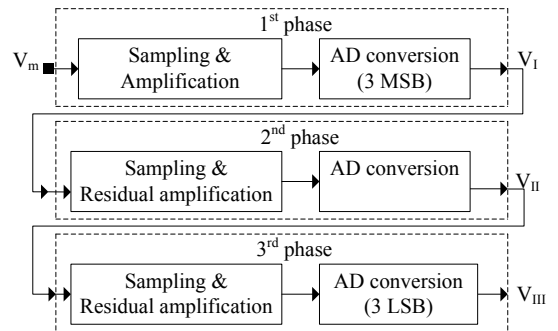


Figure 2. Conversion algorithm.

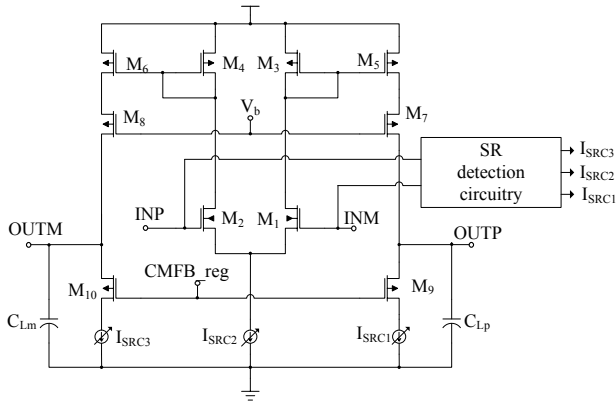


Figure 3. Operational amplifier with the slew rate detection.

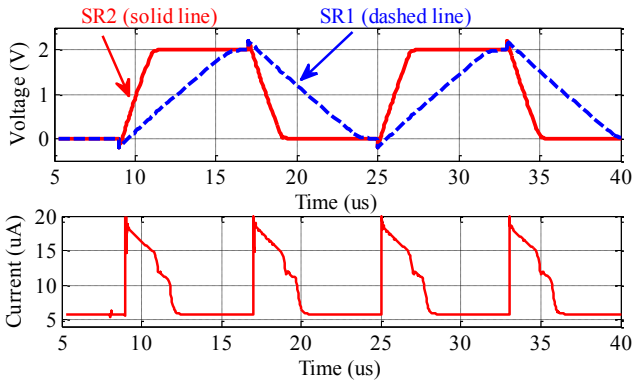


Figure 4. Slew rate and slew rate detection simulated in Cadence Spectre.

III. OPERATIONAL AMPLIFIER

In a conventional ADC, the comparator is probably the most critical part since it is directly connected to the binary-weighted capacitor array. That means that the transistors of the input differential pair of the comparator should be as small as possible since parasitic capacitances affect the division ratio and consequently ADC resolution. On the other hand small transistors in the differential pair lead to a higher offset which must be cancelled. Also, the common mode voltage must be suppressed because fluctuations of the common mode voltage can cause INL error [9], while [8] reports offset in comparators when the common voltage varies.

Although, the usage of an operational amplifier is not desirable for charge redistribution ADC due to their low speed (mostly caused by their limited slew rate) and high power consumption, there are several reasons to use an amplifier. The operational amplifier has a good suppression of common mode voltage (CMRR). Also, in the proposed ADC the comparator is directly driven by the amplifier (Fig. 1), so the parasitic capacitances are not an issue and the transistors of the input differential pair can be quite large leading to lower offset. Additionally, the kick-back noise of the dynamic comparator is attenuated by the operational amplifier.

In order to speed-up ADC performance the operational amplifier with the slew rate detection based on [10] is developed (Fig. 3). The amplifier is designed to detect slewing, turn on additional current sources (I_{SRC1} , I_{SRC2} and I_{SRC3}) during slewing and turn off current sources when slewing is over (stable state). This is the task of the SR detection circuit. The detection circuit is an auxiliary amplifier with hysteresis. During slewing the voltages at the input pins of the operational amplifier are not equal. When the difference is higher than the hysteresis of the auxiliary amplifier, additional current sources are activated and the current of the main amplifier is increased. After slewing is over, the detection circuit turns off the additional current sources and decreases the overall current consumption (Fig. 4). This actually means that the quiescent current of the amplifier can be very low, while relatively high speed is still ensured.

During slewing the currents through the amplifier (I_{SRC1} , I_{SRC2} and I_{SRC3}) are increased proportionally although, [10] [11] suggest it is not necessary. Indeed, the best case is when the maximum current charges C_{Lp} (or C_{Lm}) and discharges C_{Lm} (or C_{Lp}). In the case when current charges C_{Lp} and discharges C_{Lm} , the transistor M_9 should be turned off and M_{10} should pull maximum current. However, asymmetrical currents are causing overshoot at the amplifier outputs. The overshoots can be quite high and can degrade speed of the ADC. That is the reason why the currents in the operational amplifier are symmetrically increased. Improvement in the slew rate is shown in Fig. 4 (SR1 denotes the amplifier without the slew rate improvement, while SR2 denotes the amplifier with the slew rate detection circuit). The slew rate for SR2 is 3 times better than for SR1 (the load capacitances are $C_{Lm} = C_{Lp} = 5$ pF), and the quiescent current is slightly less than $6 \mu\text{A}$.

IV. SIMULATIONS

The proposed ADC is implemented in ON Semi $0.35 \mu\text{m}$ CMOS process and simulated in Cadence Spectre. The nominal supply voltage is 3.3 V , the nominal common mode voltage (V_{SGND}) is 1.6 V and the reference voltages V_{refp} and V_{refm} are $\pm 1 \text{ V}$ around V_{SGND} . The conversion time (including sampling and amplification of the input voltage) is $60 \mu\text{s}$. At the sampling rate of 10 kS/s the average power consumption is $33 \mu\text{W}@3.3 \text{ V}$ or $10 \mu\text{A}$ and it is dominated by the amplifier.

In RFID tags it is very hard to achieve stable voltages, so static and dynamic characteristics of the ADC are simulated when the supply voltage and reference voltage decreases with the slope of $3 \text{ mV}/\mu\text{s}$. That means that the supply voltage decreases from 3.3 V to 3.12 V during one conversion cycle of $60 \mu\text{s}$. At the same time the common voltage drops from 1.6 V to 1.42 V .

The ADC characteristics are simulated only for nominal technology parameters because of long simulation time.

A. Static characteristics

The simulated differential nonlinearity (DNL) is less than 0.53 LSB (Fig. 5) and the integral nonlinearity (INL) is less than 0.53 LSB (Fig. 6) with the 9-bit resolution.

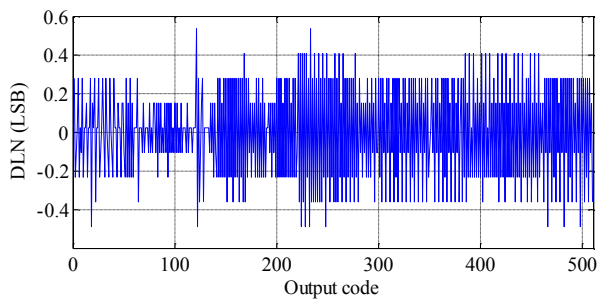


Figure 5. Differential nonlinearity (DNL) simulated in Cadence Spectre.

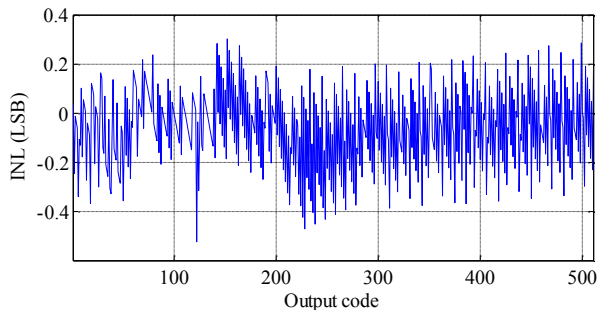


Figure 6. Integral nonlinearity (INL) simulated in Cadence Spectre.

B. Dynamic characteristics

Dynamic characteristics are simulated for a full scale 100-Hz sine wave ($2V_{pp}$) and 10 kS/s sampling rate. The signal spectrum is shown in Fig. 7. The spurious free dynamic range (SFDR) is 63 dB and signal-to-noise and distortion ratio (SNDR) is 54.2 dB. The equivalent number of bits (ENOB) is 8.7.

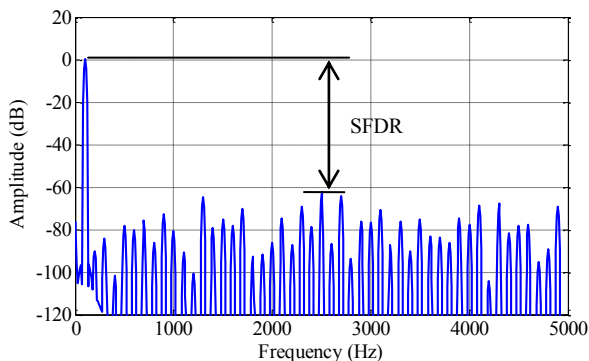


Figure 7. FFT spectrum of 100-Hz input signal at 10 kS/s (simulated in Cadence Spectre).

V. CONCLUSION

This paper presents a low-power, fully differential cyclic AD converter. It utilizes a 3-bit C-2C ladder to obtain 9-bit resolution. The conversion algorithm is presented and each phase is analyzed. For a 9-bit resolution the 3-bit C-2C ladder in the proposed ADC occupies 64 times less area than a binary weighted array. Although the operational amplifier slows down

the ADC sampling rate, there are also several benefits when using an amplifier. Since the comparator is driven by the operational amplifier, the transistors in the input differential pair of the comparator can be large. That reduces the offset voltage of the comparator caused by mismatch of the transistors. Also, kick-back noise of the dynamic comparator is attenuated by the operational amplifier. In order to minimize the amplifier consumption and speed up conversion time, the operational amplifier has the slew rate detection and control circuit. An auxiliary amplifier detects slewing and increases current in the main amplifier. After the transition is over, the current is reduced to its nominal, quiescent value. The quiescent current consumption of the operational amplifier is 6 μ A. The simulations showed that the amplifier with the slew rate detection has 3 times better slew rate than an amplifier without the slew rate detection. The total power consumption at 10 kS/s sampling rate is 33 μ W@3.3 V, i.e. the average current is 10 μ A. Simulations confirmed that the proposed ADC is insensitive to supply voltage variations, which is very important since in RFID tags it is very hard to ensure stable power supply. The simulated SFDR, SNDR and ENOB are 63 dB, 54.2 dB and 8.7 respectively. The DNL and INL are less than 0.53 LSB. The influence of the process variations and capacitor mismatch on the ADC performance will be investigated in detail in the scope of future research together with the optimization of power consumption.

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