menu

Performance Evaluation of the Hilbert Transform Based Digital Phase-Locked Loop

Ivica Kopriva and Dragan Juricic
Institute for Defense Studies, R&D, Bijenicka 46, 10000 Zagreb, Croatia
e-mail: ivica.kopriva@public.srce.hr, dragan.juricic@public.srce.hr

Abstract

Multiplier free Digital Phase-Locked Loop (*DPLL*) based on Hilbert transform has been analyzed in this paper. The performance of this DPLL when applied as FM demodulator is evaluated in relation to the DPLL with Multiplier based Phase Detector (MPD) showing better dynamic properties expressed in the form of the lock range, settling time, pull-out range etc.

1. Introduction

In the field of communication, the phase-locked loop (*PLL*) is frequently used for frequency demodulation [1],[2]. In analog PLL and appropriate variant of the DPLL, the analog and digital multipliers are used as Phase Detectors (*PD*). The MPD measures the phase difference between the input and output signals and produces an error signal proportional to the measured phase difference. The output signal of the MPD consists of a DC component (*phase difference*) and an unwanted AC component (*high frequency component*). The Low Pass (*LP*) filter in the loop removes the AC component of the MPD. The loop filter transfer function has an important influence on the dynamic performance of the loop. If we want to use the PLL to demodulate frequency modulation the loop filter must be wide enough to obtain best loop tracking and acquisition properties, or the loop bandwidth should be made as large as possible to minimize phase error. Simultaneously, the loop filter should reject undesired high frequency component of the MPD and it must be chosen as LP filter. It can be shown that if cuttoff frequency of the loop filter is too low and the frequency deviation of the input FM signal is excessive, the PLL can lose lock. Actually, there is a conflict in design of the loop filter and desired dynamic features of the PLL [3].

2. Hilbert transform PD

The Hilbert Transform based Phase Detector (*HTPD*), which employs quadrature signal processing method [4], estimates phase difference between input and output signals without using LP filter:

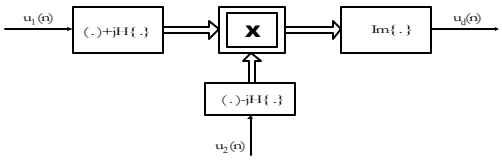

Figure 1: HTPD operating principle

This PD extracts the phase error between the input $\boldsymbol{u_1(n)}$ and output $\boldsymbol{u_2(n)}$ signals of the PLL by complex multiplication of complex signals [5],[6],[7]. A complex signal of the form $\boldsymbol{u(n) \pm j\,\tilde{u}(n)}$ is synthesized from a real signal $\boldsymbol{u(n)}$ and its Hilbert Transform and is known as an analytic signal. The input and output analytic signals of the PLL are defined by:

$$U_1(n) = u_1(n) + j\hat{u}_1(n) = A_1 e^{j[w_0 n + j_1(n)]}$$
$$U_2(n) = u_2(n) - j\hat{u}_2(n) = A_2 e^{j[w_0 n + j_2(n)]} \quad (1)$$

The complex multiplication of these analytic signals produces an output analytic signal of the PD. The real signal of the PD can be obtained by taking imaginary part of this analytic signal:

$$u_d(n) = IM\{A_1 A_2 e^{j[j_1(n) - j_2(n)]}\} = \\ = A_1 A_2 \sin[j_1(n) - j_2(n)] = A_1 A_2 \sin[j_e(n)] \quad (2)$$

It can be seen that the output signal of the HTPD $u_d(n)$ consists of a DC component and does not contain the unwanted AC component. Consequently, there is no need for using a LP filter as a PLL component building block. The digital controlled oscillator (*DCO*) used in this type of PLL generates two signals, an in-phase signal I and a quadrature signal Q. The DCO is not able to compute I and Q signals directly. These signal are calculated indirectly from the phase $f_2(n)$. I signal and Q signals are the Hilbert-transform pair. The signal flow diagram for this DPLL is illustrated in Fig. 2.

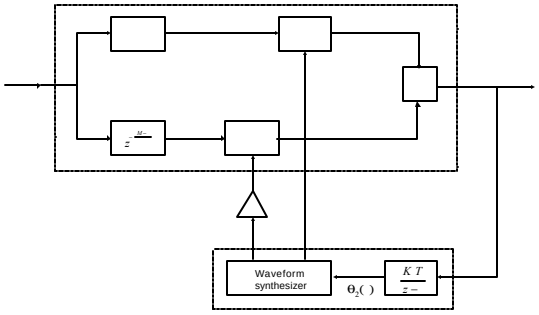

Figure 2. The digital PLL with HTPD

As indicated in the block diagram, this type of DPLL is a first-order loop because the loop filter is omitted. The loop delays input signal by (*M-1)/2* time steps and the output signal of HTPD directly controls the DCO.

3. Performance analysis

Performance of the DPLL with HTPD is compared with the DPLL with MPD through evaluation of the four key parameters specifying frequency range in which PLL can be operated. The loop filter has an important influence on these parameters. They are defined for both variants of the loop as:

	Digital PLL with LP filter	**Digital PLL with HTPD**
The hold range (Δw_H)	$K_o K_d H(0) \to \infty$	$K_o K_d$
The lock range (Δw_L)	$\frac{K_o K_d t_2}{t_1} = 2w_n x$	$K_o K_d$
The pull-out range (Δw_{PO})	$\approx 1.8 w_n (x+1)$	$K_o K_d$
The pull-in range (Δw_P)	$\to \infty$	$K_o K_d$

where w_n is the loop natural frequency, K_d is gain of PD and K_0 is gain of the VCO. If, the PLL is pulled-out by a large frequency step, we can expect that PLL to come back to stable operation. This process is known as pull-in process and is relatively slow. The frequency step which causes loop to lose lock, is much greater for the PLL with HTPD than the PLL with MPD. The DPLL with HTPD has larger lock range than a DPLL with MPD and is able to track faster phase and frequency variations of the input signal. Moreover, the loop bandwidth for the DPLL with HTPD is greater than the DPLL with MPD as follow:

The loop bandwidth	DPLL with LP filter	DPLL with HTPD
w_g	$w_g \approx w_n = \sqrt{\frac{K_o K_d}{t_1}}$	$w_g \approx K_o K_d$

It is clear that the loop filter reduces the loop bandwidth. Consequently, the lock-in time (*settling time*) for the PLL with HTPD is very short.

One of the main advantages of using the PLL is its ability to demodulate and track signal in noise. The PLL offers excellent noise immunity compared to other designs [8],[9]. When noise is superimposed on input signal loop bandwidth must be as narrow as possible to minimize output phase jitter. Whereas, the loop bandwidth should be made as large as possible to obtain best tracking and acquisition properties [1]. Than, there is a problem when we try to choose appropriate parameters of the loop. The output signal-to-noise ratio SNR_{out} versus the input signal-to-noise ratio SNR_{in} curve characterizes the PLL FM demodulator performance in the presence of noise. To calculate the signal-to-noise ratio of the VCO output SNR_{out}, it is necessary to know the SNR_{in}, the noise bandwidth of the loop B_L and the input noise bandwidth B_i as follow [3]:

$$SNR_{out} = \frac{B_i}{B_L} SNR_{in} \qquad (3)$$

If the input bandpass filter is considered as a part of the PLL FM demodulator the noise bandwidth B_i is the bandwidth of such a filter. The noise bandwidth of the loop for both types of the PLL design is defined as [3],[10]:

	Digital PLL with LP filter	Digital PLL with HTPD
The loop bandwidth [Hz]	$B_L = \frac{w_n}{2}\left(z + \frac{1}{4z}\right)$	$B_L = \frac{K_d K_o}{4}$

The PLL with HTPD has larger noise bandwidth of the loop than digital PLL with multiplier PD. Thus, this PLL has less rejection of the noise superimposed on input signal. In practice, when PLL is used as FM demodulator we must filter the output signal for both variants of the PLL design. The rectangular passband postfilter with cuttoff frequency equal to the massage bandwidth should be used [9]. Therefore, these demodulators have approximately equal noise performance when the postfilter is used.

4. Simulation results

In this paper, we simulated behavior of the digital PLL with the MPD and digital PLL with HTPD. The loops are implemented by software on DSP TMS320C40 (TI) in real time [11]. First loop (PLL with MPD) is the ordinary second–order loop with the active loop filter and flat amplitude response $z = 0.70$ (*damping factor*). The special 80^{th}-order FIR filter is used as Hilbert transformer in the second loop. The loops are designed in order to demodulate a real FM signal which has the center frequency $f_C = 22.5\,kHz$, the frequency deviation $\Delta f = 10\,kHz$, the modulation frequency $f_m = 75\,Hz$ and amplitude $A_1 = 1V$. The sampling frequency is 100 kHz.

$$u_1(t) = A_1 \sin\left[2\pi f_c t + \frac{\Delta f}{f_m}\sin(2\pi f_m t)\right] \qquad (4)$$

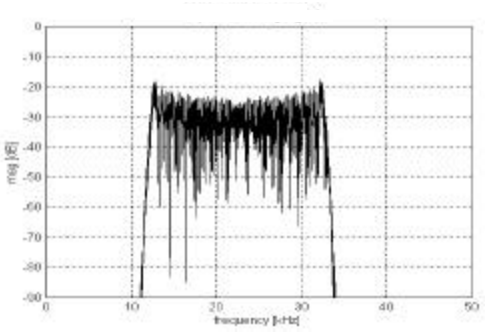

Figure 3. The spectrum of the input signal

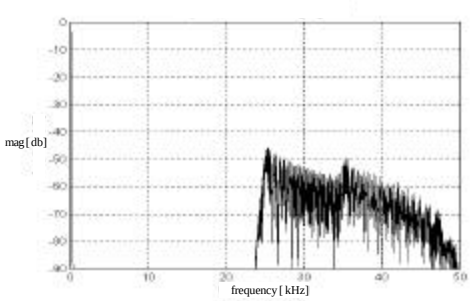

Figure 4. The spectrum of demodulated signal (the PLL with MPD)

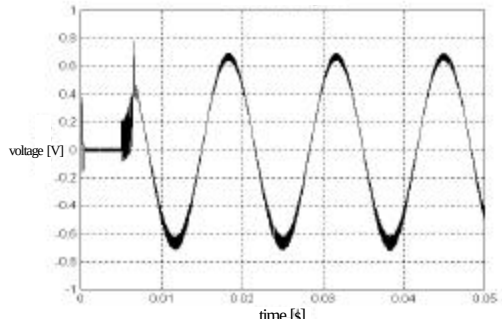

Figure 5. The demodulated signal

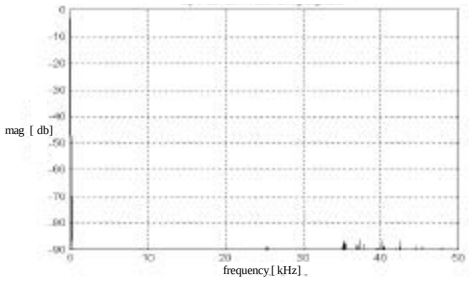

Figure 6. The spectrum of demodulated signal (the PLL with HTPD)

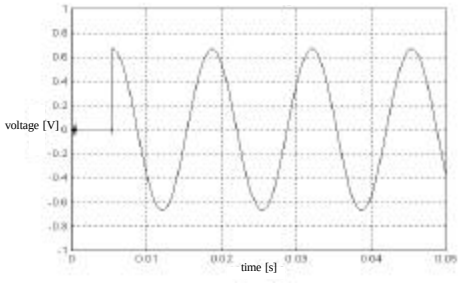

Figure 7. The demodulated signal

As illustrated (Fig.6), the output signal of the PLL with HTPD does not contain the unwanted AC component near frequency $2f_c$, contrary to the digital PLL with MPD (Fig. 4). When we want to design the digital PLL with MPD we must choose the parameters ζ and ω_n, which determine the frequency response and the phase error of the loop. Whereas, the phase error depends on frequency deviation Δf and modulation frequency f_m of the input FM signal [1]. The phase error must be small and lie within the linear range of the loop all the time. In that case, demodulating signal is reproduced at the loop output with minimum distortion [8]. For greater modulation frequency which is equal to $f_m = 750\,Hz$ but still smaller than the loop bandwidth, this PLL will lose lock (Fig. 8 and 9). The PLL with HTPD has larger loop bandwidth and can track the new modulation frequency of the input signal. Generally, there is no tracking problem for this PLL when the input frequency lies in the hold range of the loop (Fig. 10 and 11).

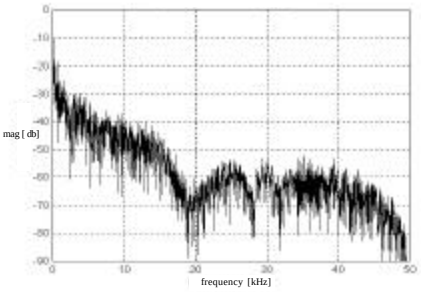

Figure 8. The spectum of demodulated signal (the PLL with MPD)

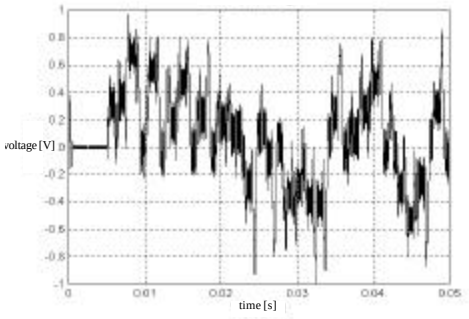

Figure 9. The demodulated signal

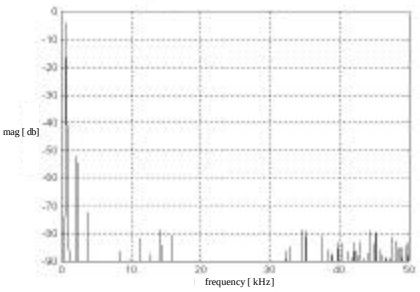

Figure 10. The spectrum of demodulated signal (the PLL with HTPD)

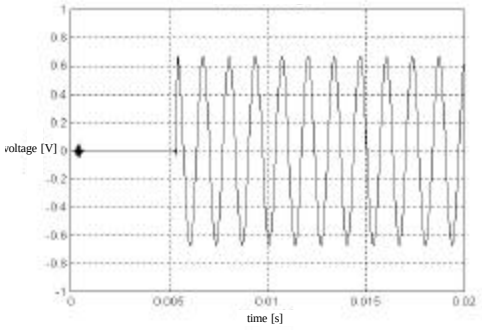

Figure 11. The demodulated signal

5. Conclusions

The design of digital PLL as FM demodulator with HTPD and the main results of the performance analysis are presented in this paper. The computational operations required for this PLL suggest implementation by software. The key element of this PLL is the HTPD which extracts the phase error by mathematical computations without using a LP filter. Consequently, this PLL has larger bandwidth, pull-out and lock range than digital PLL with MPD. Therefore, it is able to track faster frequency variations of the input signal which instantaneous frequency lies in the hold range of the loop. This PLL has less rejection of the noise superimposed on the input signal due to the larger noise bandwidth of the loop. The output signal of the loop is delayed by (M-1)/2 time steps because the ideal Hilbert transformer is realized as FIR structure [6],[7]. The sampling frequency must be at least twice the highest-frequency component existing in input signal [12].That is not case for the PLL with MPD where the sampling frequency must be at least four time greater than the highest-frequency component existing in input signal. Whereas, the software algorithm for this PLL is more complicated than algorithm of the PLL with MPD.

References

[1] B.T. Mills, "The Phase Locked Loop as a Communication System Building Bock", NS Application Note 46, June 1971.

[2] H.Taub, D.L. Schilling, "Principles of Communication Systems", McGRaw-Hill, 1987.

[3] R. Best, "PLL-Theory, Design and Applications", McGraw-Hill, 1993.

[4] P. Gerdsen, P. Kroeger, "Digitale signalverarbeitung in der Nachrichten-ubertragung", Springer- Verlag,1993.

[5] S. Haykin, "Communication Systems", John Wiley & Sons, 1994.

[6] L. R. Rabiner, B. Gold,"Theory and Application of Digital Signal Processing", Prentice-Hall, 1975

[7]J. G. Proakis, D. G. Manolakis, "Introduction to Digital Signal Processing", Macmillan Publishing Company, 1989

[8] R. Volgers, "Phase Locked Loop Circuits, Philips Components", 1989.

[9] P. Hasan, "PLL FM Demodulator Performance Under Gaussian Modulation", IEEE Trans. Commun., vol. COM-46, pp.437-440, April 1998.

[10] P. Z. Peebles, "Probability, Random Variables and Random Signal Principles", McGraw -Hill, 1993.

[11] TMS 320C40 User's Guide-Texas Instruments,1996.

[12] D.Robertson, "Selelcting Mixed-Signal Components for Digital Communications systems" Part V, Analog Dialogue 31-3 (1997.)