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Estimation Error of Semiconductor Device's Virtual Junction Temperature in IEC's Approximate Formula

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Original scientific paper

Diagrams were devised which enable a determination of errors in estimating the virtual junction temperature of semiconductor devices for a long train of equal amplitude rectangular load power pulses with the IEC-recommended approximate formula. They show that for no semiconductor device the estimation error for virtual junction temperature with IEC-recommended approximate formula exceeds a certain value. IEC's conditions for good approximation proved unnecessary.

Key words: semiconductor devices, thermal calculation, virtual junction temperature

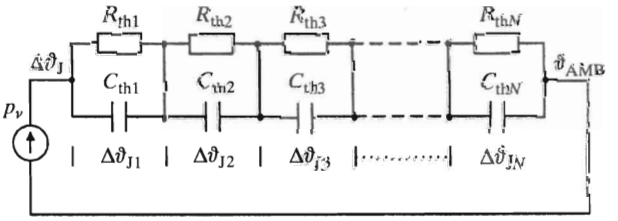
1 INTRODUCTION

In 1973 IEC Publication 146 [1] referred to the possibility of using the calculation method for instantaneous maximum virtual junction temperature of diodes and thyristors loaded by a long train of equal amplitude rectangular power pulses on qualitative condition that temperature excursion above the average temperature should remain low compared with the average temperature. The same year, IEC Publication 147-2E [2] defined conditions for a satisfactory accuracy of the method, leaving, however, its accuracy unquantified. In 1983, the method was recommended unchanged in another IEC Publication 747-2 [3]. In 1989 discussions about a revision of IEC Publication 146 ended with the revision appearing in 1991 as Technical Report 146-1-2 [4]. This time, through, there was no mention of conditions for the method's satisfactory accuracy.

This method of estimating virtual junction temperature of diodes and thyristors was authored by Gutzwiller and Sylvan already in 1961 [5]. Interestingly, they stated that, unfortunately without giving a proof, the method was »usually accurate within 3 %«.

2 THE ACCURATE AND THE APPROXIMATE FORMULA FOR ESTIMATING MAXIMUM VIRTUAL JUNCTION TEMPERATURE

It was shown in [5] that the transient function of the thermal system of a semiconductor device can be approximated with sufficient accuracy by a finite sum of exponential functions. This fact had led to the development of the electrical model of the semiconductor device thermal system shown in Figure 1. In it, electrical resistors and capacitors are analogous to a thermal resistors and capacitors. Current is analogous to input power losses and voltage at model inputs is analogous to a temperature difference between semiconductor device's silicon and the environment.



$$z_{th} = \sum_\nu z_{th\nu} \qquad z_{th} = \sum_\nu R_{th\nu}(1-e^{-t/\tau_{th\nu}})$$

$$\tau_{th\nu} = R_{th\nu}C_{th\nu} \qquad \tau_{th1} < \tau_{th2} < \ldots < \tau_{thN}$$

Fig. 1 Electrical model of a semiconductor device's thermal system

The response of the electrical model of semiconductor device's thermal system to a set arbitrary load is calculated using the superposition principle. It requires the asumption that the thermal system of a device is linear, and the knowledge of the electric model given in Figure 1. Different methods (analytical, graphoanalytical and numeric) may be used in arriving at the final result, namely, at the virtual junction temperature of the semiconductor device. In the case of a load with constant pulse losses of rectangular waveform, the analytical estimation method produced the following formula for the calculation of the stationary maximal virtual junction temperature

$$\left[\Delta\vartheta_{J(st)}(\kappa_1)\right]_{\text{accur}} = P_{VM}\sum_{\nu=1}^{n} R_{th\nu}\frac{1-\mathrm{e}^{-\frac{\kappa_1}{\tau_{th\nu}}}}{1-\mathrm{e}^{-\frac{T}{\tau_{th\nu}}}} \qquad (1)$$

where

$\Delta\vartheta_{J(st)}(\kappa_1)$ is the maximal virtual junction temperature for stationary state, K

$R_{th\nu}$ is thermal resistance of the νth RC-pair in the electrical model of the semiconductor device thermal system, K/W

P_{VM} is loss amplitude, W

$\tau_{th\nu}$ is a time constant of the νth RC-pair in the electrical model of the semiconductor device thermal system, s

κ_1 is pulse loss duration, s

T is period of pulse losses, s

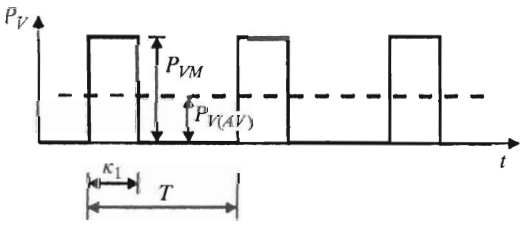


Fig. 2 Constant pulse losses of rectangular waveform

A disadvantage to using analytical calculation method is that it requires adding of individual RC-pair contributions. It was one of the reasons why IEC suggested the approximate formula to calculate the maximal silicon virtual junction temperature for load, as in Figure 2. The formula was derived from the graphoanalytical method and from the so-called »two pulse« approximation, Figure 3.

$$\left[\Delta\vartheta_{\theta J(st)}(\kappa_1)\right]_{\text{approx}} = P_{VM}\left[\delta R_{th} + (1-\delta)z_{th}(T+\kappa_1) - z_{th}(T) + z_{th}(\kappa_1)\right] \qquad (2)$$

where

R_{th} is total thermal resistance of semiconductor device's thermal system, K/W

δ is duty factor $(=\kappa_1/T)$

z_{th} is semiconductor device's transient thermal impendance for constant current, K/W

Employing formula (2) produces a quicker result. It is conservative, however, since it approximates a periodic sequence of rectangular pulse losses with constant losses $P_{V(AV)}$ till the penultimate pulse. Its conservativeness is capable of being determined by seeking the percentage of absolute error of virtual silicon junction temperature estimation $P_{VM}R_{th}$.

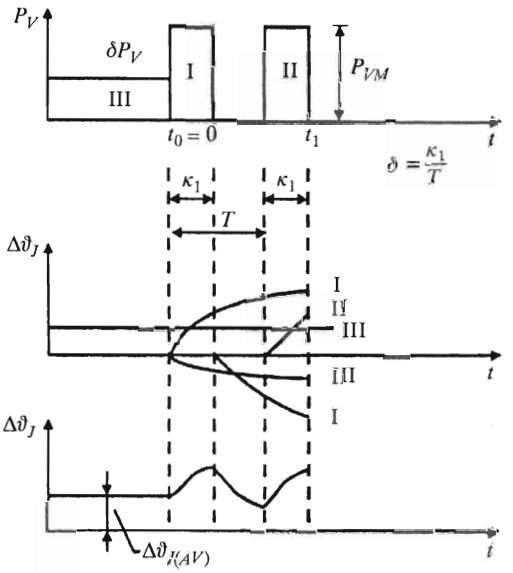


Fig. 3 A graphoanalytical method explanation for the estimation of virtual junction temperature by »two pulse« approximation

3 THE SIZE OF ESTIMATION ERROR IN SEMICONDUCTOR DEVICE'S VIRTUAL JUNCTION TEMPERATURE

Let the estimation error be defined as

$$e_r = \frac{\left[\Delta\vartheta_{J(st)}(\kappa_1)\right]_{\text{approx}} - \left[\Delta\vartheta_{J(st)}(\kappa_1)\right]_{\text{accur}}}{P_{VM}R_{th}} \qquad (3)$$

respectively

$$e_r = \frac{\sum_{\nu}\left[\Delta\vartheta_{J(st)\nu}(\kappa_1)\right]_{\text{approx}} - \sum_{\nu}\left[\Delta\vartheta_{J(st)\nu}(\kappa_1)\right]_{\text{accur}}}{P_{VM}\sum R_{th}} \qquad (4)$$

By developing (4) it follows

$$e_r = \frac{\left\{\left[\Delta\vartheta_{J(st)1}(\kappa_1)\right]_{\text{approx}} - \left[\Delta\vartheta_{J(st)1}(\kappa_1)\right]_{\text{accur}}\right\}}{P_{VM}R_{th}} + \frac{\left\{\left[\Delta\vartheta_{J(st)2}(\kappa_1)\right]_{\text{approx}} - \left[\Delta\vartheta_{J(st)2}(\kappa_1)\right]_{\text{accur}}\right\}}{P_{VM}R_{th}} + \ldots \qquad (5)$$

or

$$e_r = \frac{\left[\Delta\vartheta_{J(st)1}(\kappa_1)\right]_{\text{approx}} - \left[\Delta\vartheta_{J(st)1}(\kappa_1)\right]_{\text{accur}}}{P_{VM}R_{th}} \cdot \frac{R_{th1}}{R_{th}} + \frac{\left[\Delta\vartheta_{J(st)2}(\kappa_1)\right]_{\text{approx}} - \left[\Delta\vartheta_{J(st)2}(\kappa_1)\right]_{\text{accur}}}{P_{VM}R_{th}} \cdot \frac{R_{th2}}{R_{th}} + \ldots \tag{6}$$

The final result may be shown as

$$e_r = \sum_{\nu} e_{r\nu} \frac{R_{th\nu}}{R_{th}} \tag{7}$$

where

$$e_{r\nu} = \delta \cdot \mathrm{e}^{-\left(1+\frac{1}{\delta}\right)\frac{\kappa_1}{\tau_{th\nu}}} - \mathrm{e}^{-\frac{2}{\delta}\frac{\kappa_1}{\tau_{th\nu}}} \cdot \frac{1-\mathrm{e}^{-\frac{\kappa_1}{\tau_{th\nu}}}}{1-\mathrm{e}^{-\frac{2}{\delta}\frac{\kappa_1}{\tau_{th\nu}}}} \tag{8}$$

Error $e_{r\nu}$ is a function of the duty factor $\delta = \kappa_1/T$, and of the proportion $\kappa_1/\tau_{th\nu}$. From physical quantities both in the first and second ratio, it follows that error $e_{r\nu}$ is a function of input power losses and of semiconductor device's thermal system. Figure 4 shows error diagram $e_{r\nu}$, with duty factor δ as a parameter. Function (8) reaches its maximum at $\delta = 0.4445$ and $\kappa_1/\tau_{th\nu} = 0.2983$, amounting to $e_{r\nu} = 0.0308$.

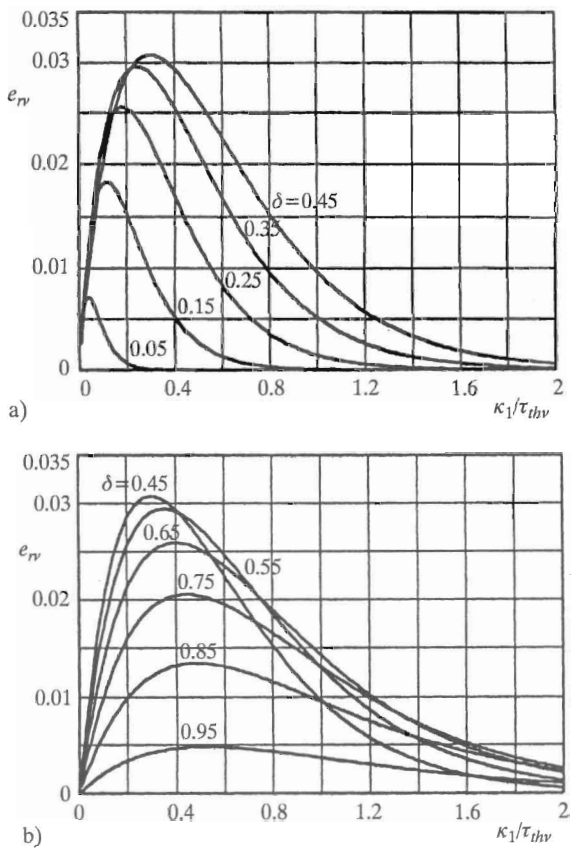


Fig. 4 Virtual junction temperature estimation error in vth RC-pair of the electrical model of semiconductor device's thermal circuit when using IEC-recommended formula: a) $\delta \le 0.45$; b) $\delta \ge 0.45$

From the above values of these parameters and the assumption that semiconductor device's thermal system is replacable by one RC-pair it can be inferred that maximum error e_r equals 3.08 % $P_{VM}R_{th}$.

4 CONDITIONS FOR A SMALL ESTIMATION ERROR IN THE SEMICONDUCTOR DEVICE'S VIRTUAL JUNCTION TEMPERATURE

Since the estimation error $e_{r\nu}$ reaches a maximum both according to δ and $\kappa_1/\tau_{th\nu}$, Figure 5, four conditions may be set to keep it low

$$\kappa_1/\tau_{th\nu} > \mathrm{a}_1 \tag{9}$$

$$\kappa_1/\tau_{th\nu} < \mathrm{a}_2 \tag{10}$$

$$\delta > \mathrm{a}_3 \tag{11}$$

$$\delta < \mathrm{a}_4 \tag{12}$$

where a_1, a_2, a_3 and a_4 are real constants. Of these four, IEC mentions two. It is stated in its recommendations that the estimation error is small »if one of the following conditions is fullfilled«

$$z_{th}(\kappa_1) > 0.5\, R_{th} \tag{13}$$

$$z_{th}(T) - z_{th}(\kappa_1) < 0.1\, R_{th} \tag{14}$$

It was shown that condition (13) meets condition (9), and condition (14) condition (11). Nonequation (13) represents a condition for $\kappa_1/\tau_{th\nu}$, i.e., for the device's thermal system; nonequation (14) states the condition for κ_1/T, i.e., for device's losses.

a) Condition $z_{th}(\kappa_1) > 0{,}5\, R_{th}$

This condition, expressed by parameters of the electrical model of the semiconductor device's thermal circuit, takes this shape

$$\sum_{\nu} R_{th\nu}\left(1-\mathrm{e}^{-\frac{\kappa_1}{\tau_{th\nu}}}\right) > 0.5 R_{th} \tag{15}$$

It follows

$$\sum_{\nu}\frac{R_{th\nu}}{R_{th}} - \sum_{\nu}\frac{R_{th\nu}}{R_{th}}\mathrm{e}^{-\frac{\kappa_1}{\tau_{th\nu}}} > 0.5 \tag{16}$$

respectively

$$\sum_{\nu}\frac{R_{th\nu}}{R_{th}}\mathrm{e}^{-\frac{\kappa_1}{\tau_{thN}}\cdot \mathrm{a}_{\nu}} < 0.5 \tag{17}$$

a_ν being ratio of the largest time constant τ_{thN} to νth time constant $\tau_{th\nu}$. This condition requires a sufficiently large κ_1 compared with, say, the largest time constant τ_{thN} of the electrical model of the semiconductor device's thermal circuit. This means that the last loading pulse is the one primarily determining the virtual junction temperature, condition that is also understandable from equation (2) and Figures 4, 5.

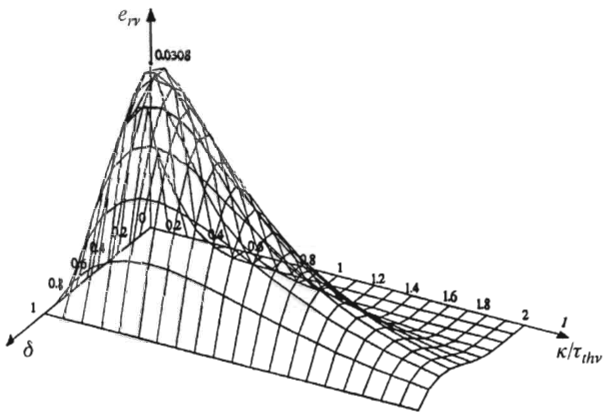


Fig. 5 Error in virtual junction temperature estimation of νth RC-pair of the electrical model of device's thermal circuit when using IEC-recommended formula as a function of two variables: δ and $\kappa_1/\tau_{th\nu}$

b) Condition $z_{th}(T) - z_{th}(\kappa_1) < 0.1\, R_{th}$

In terms of parameters of the electrical model of the semiconductor device's thermal circuit this condition may be expressed

$$\sum_\nu R_{th\nu}\left(1 - e^{-\frac{T}{\tau_{th\nu}}}\right) - \sum_\nu R_{th\nu}\left(1 - e^{-\frac{\kappa_1}{\tau_{th\nu}}}\right) < 0.1\, R_{th} \quad (18)$$

It follows

$$\sum_\nu \frac{R_{th\nu}}{R_{th}}\left(1 - e^{-\frac{T}{\tau_{th\nu}}}\right) - \sum_\nu \frac{R_{th\nu}}{R_{th}}\left(1 - e^{-\frac{\kappa_1}{\tau_{th\nu}}}\right) < 0.1 \quad (19)$$

namely

$$\sum_\nu \frac{R_{th\nu}}{R_{th}}\left[e^{-\frac{\kappa_1 \cdot a_\nu}{\tau_{thN}}} - e^{-\left(\frac{1}{\delta}\right)\left(\frac{\kappa_1 \cdot a_\nu}{\tau_{thN}}\right)}\right] < 0.1 \quad (20)$$

This condition stipulates that δ must be sufficiently large. This means that maximum virtual junction temperature is mainly determined by average losses. The condition is evident from Figure 4, for $\delta > 0.45$ the estimation error $e_{r\nu}$ is smaller. It is also clear from Figures 4, 5 that this condition is very loose, because the maximum of function $e_{r\nu}(\kappa_1/\tau_{th\nu}, \delta)$ falls slowly with the rise of δ. Only above $\delta = 0{,}7$ does the error become noticeably smaller.

c) Discussion of conditions

Conditions (15) and (18) obviously exclude the majority of loads seen in practice. Condition (15) requires κ_1 to be greater than approximately $0.4\,\tau_{thN}$. Condition (18) demands a δ greater than about 0.7.

The way the conditions (15) and (18) act in an imaginary semiconductor device having the following transient thermal impendance

$$\frac{z_{th}(t)}{R_{th}} = 0.1\left(1 - e^{-\frac{t}{\tau_{thN}}a_1}\right) + 0.2\left(1 - e^{-\frac{t}{\tau_{thN}}a_2}\right) + 0.7\left(1 - e^{-\frac{t}{\tau_{thN}}a_3}\right) \quad (21)$$

is shown in Figure 6. It, e.g., makes it clear that in the absence of limiting conditions estimation error e_r attains a maximum of 0.027 (Figure 4a); with the

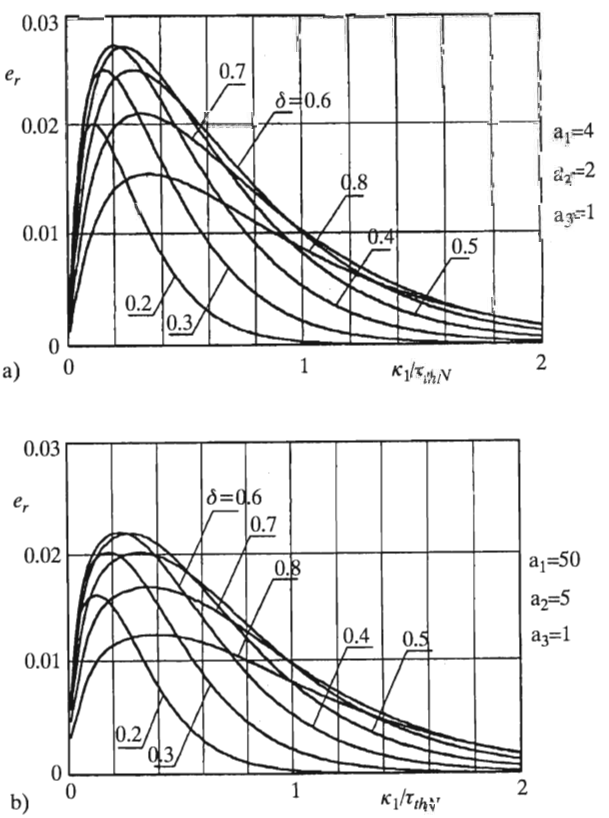


Fig. 6 Estimation error in virtual junction temperature when using the IEC-recommended formula for an imaginary device with transient thermal impedance according to equation (21)

limiting conditions (15) and (18) the respective maximums are 0.022 and 0.015 (Figure 6b).

Mathematical expression (21) was arrived and based on an analysis of catalog data on transient thermal impendance for more than 300 diodes and thyristors from different manufacturers by assuming the number of RC-pair and R_{thv} parameter values producing an estimation error e_r equal to, or greater than of real semiconductor devices.

5 CONCLUSION

An error in estimating a semiconductor device's virtual junction temperature using the IEC-recommended formula for any semiconductor device whose transient thermal impedance may be expressed mathematically by a sum of exponential functions is less than $0.308\ P_{VM}R_{th}$. Under the IEC conditions for the application of the recommended formula, this error is limited to $0.022\ P_{VM}R_{th}$ in the present commercial diodes and thyristors. Since the conditions for the recommended formula's application restrict its field of application without simultaneously substantially improving the accuracy of the estimation, one would be justified if he dropped from future IEC documents references to conditions for the recommended formula's applicability.

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Pogreška proračuna nadomjesne temperature silicija poluvodičkih komponenata uporabom IEC-ove približne formule. Izračunati su dijagrami koji za određivanje pogreške proračuna nadomjesne temperature silicija poluvodičkih komponenata opterećenih periodičnim nizom pravokutnih impulsa gubitaka uporabom IEC-ove preporučene približne formule. Oni pokazuju da niti kod jedne poluvodičke komponente pogreška proračuna nadomjesne temperature silicija ne prekoračuje određenu vrijednost. Pokazano je da su IEC-ovi uvjeti zadavoljavajuće točnosti IEC-ove preporučene približne formule nepotrebni.

Ključne riječi: poluvodičke komponente, toplinski proračun, nadomjesna temperatura silicija

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