

Usage of a three-level neutral-point clamped inverter in electric traction applications

Marinko Kovačić, Ivan Mrčela, Viktor Šunde, Željko Jakopović
University of Zagreb, Faculty of Electrical Engineering and Computing
Department of Electric Machines, Drives and Automation

Abstract—This paper analyzes the possibilities of applying a diode-clamped three-level inverter (NPC - neutral point clamped) in electric traction. This possibility was analyzed by simulating a traction profile of an electric tram. A computer program enabling comparison between different topologies, modulation strategies and control laws was made to conduct the simulation. The model used in the simulation is based on the averaged model of the three-level inverter. The model is averaged within one switching period. Semiconductor losses can be determined using the data from various semiconductor vendors and can be included in the averaged model. Temperature increase of each of the switches in the converter are determined, based on the known thermal model of the semiconductor module. The three-level converter is compared to the two-level one based on the data acquired via simulation. Some possible further investigations are suggested based on the advantages and disadvantages of the three-level topology.

Keywords—three-level inverter, averaged model, electric traction, semiconductor loss modelling, semiconductor thermal model, lifespan.

I. INTRODUCTION

Recent research is leaning towards the use of multilevel inverters of various topologies. These inverters are used in various industrial applications. The (classic) two-level topology is currently the most commonly used topology in the industry: renewable energy sources, electric propulsion systems, electric traction and anywhere where the industry requires adjustable speed drives. That type of converter and its topology are well known and thoroughly explored. A great number of vendors offer ready-made modules (IGBTs are the most common switches) and they are getting cheaper by the day.

Multilevel inverters have been used mostly in mid-voltage applications, especially in high-power drives [1]. Trends in development of renewable energy sources and constant increase in power available from windmills and photovoltaics are contributing to the increased demand for power converters. Inverters are usually used as a link between the renewable energy source and the power grid. Multilevel topologies are frequently used in such applications, mostly because of the low price-to-performance ratio [2]. The inherent low THD (total harmonic distortion) of the multilevel topologies' output voltage is their main advantage while connecting the power source to the existing grid. This feature is very important while connecting any power source to the grid. The output filter can be designed significantly smaller, volume-wise, with the use of multilevel converters. This is an advantage, since the filter is now cheaper to make. Another important advantage is the reduced acoustic noise within the audible range [3]. This is

a feature which is very important if using the inverter in a non-industrial environment, such as electric vehicles, elevators, renewable energy sources attached on housing buildings, etc.

Ready-made power modules adjusted for some three-level topologies have been produced for the past few years, mostly thanks to the increased demand for multilevel inverters in the renewable energy segment. Most of the world's largest vendors (*Infineon, Semikron, Powerex, Mitsubishi, Vincotech, Danfoss...*) offer ready-made phase legs of a three-level inverter.

Several papers investigate the use of a three-level NPC inverter in electric traction. Dieckerhoff considers using cascaded multilevel converters as a part of an electric train drive, operating at 15 kV [4]. Teichmann compares a two- and three-level NPC inverter in low-voltage devices used in industrial applications and electric traction [5]. These papers don't consider the complete drive profile of the electric vehicle, but rather only the critical operating points (maximum load point).

The paper presents a method for quick simulation of an electric drive system used in electric traction. This method enables the complete driving profile simulation and acquiring specific data (e.g. separate switch losses, semiconductor temperature rise, DC link voltage, various motor-related data...).

II. THREE-LEVEL NPC INVERTER

Since the basics of Pulse Width Modulation (PWM) of a three-level inverter are thoroughly described in [6], this paper focuses on the role this type of converter has as a part of an electric system (specifically, as a part of an electric traction system). The detailed basics of operation are out of the paper's scope.

Picture 1 shows the topology of a three-level NPC inverter. Each of the three legs consists of a four controllable semiconductor valves, e.g. IGBTs or GTOs, and six diodes. Diodes D_5 i D_6 connect the leg output with the DC link common point.

Two carrier signals, upper and lower, modulate the control signals for all three phases of the converter, D_1 , D_2 and D_3 . Control signals for the pair of complementary transistors T_1 and T_3 are generated comparing the reference signal with the carrier signal. Control signals for the pair of complementary transistors T_4 and T_2 are generated comparing the same reference signal as for the previous pair of transistors with the lower signal carrier, as presented on picture 2. Table I shows three possible levels of the output phase voltage. Picture 2 shows the phase-to-phase voltage waveform. The line-to-line

Table I. OUTPUT VOLTAGES STATES

T ₁	T ₂	T ₃	T ₄	U_{1N}
1	1	0	0	$+\frac{U_{DC}}{2}$
0	1	1	0	0
0	0	1	1	$-\frac{U_{DC}}{2}$

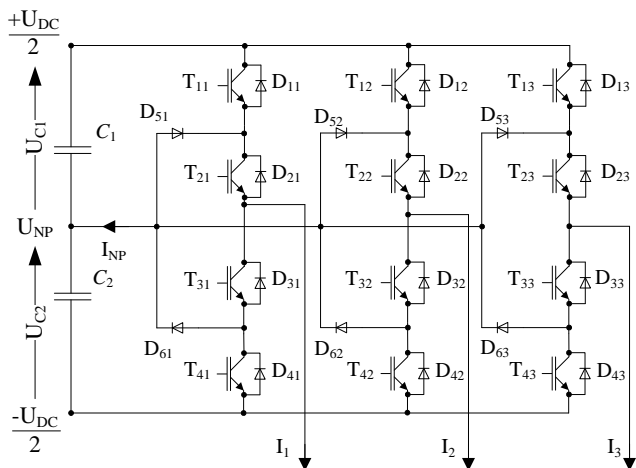


Figure 1. A neutral-point clamped three-level inverter

output voltage has five levels, with the top level being the full DC link voltage.

Controllable switches (transistors) switch only within one-half period, instead of the whole period. In addition, the turn-on and turn-off voltage stress of the switches is only half of the DC link voltage. These two facts combined make for the greatest advantage of the three-level topology compared to the two level one - lower switching loss at higher frequencies.

The output voltage range is identical as in the two-level case. It can be expanded using the same methods (e.g. Space Vector Modulation - SVM, Hybrid Space Vector Modulation - HSVM, Discontinuous Pulse Width Modulation - DPWM, ...).

III. ELECTRIC DRIVE EMPLOYED IN TRACTION SIMULATION PROGRAM

One of the more important parts is to conduct a set of simulations needed to analyze the use of different inverter topologies in electric traction. Since the inverter is operating in all operation scenarios: acceleration - the drive is acting as a motor and deceleration - the drive is acting as a generator, simulating the inverter operating as a part of such a drive is fairly complex. The duration of the simulation itself is also a limiting factor, since the duration of such simulation profiles is often measured in minutes. The simplest way to simulate this converter would be to use the switching model. Simulations using the switching model are, however, very time and resource consuming.

The solution was to use the averaged model. This chapter describes the basic concepts in the simulation used in this paper. Components which can be analyzed for themselves are separated from the drive as a whole. Picture 3 depicts the block structure of the simulation program.

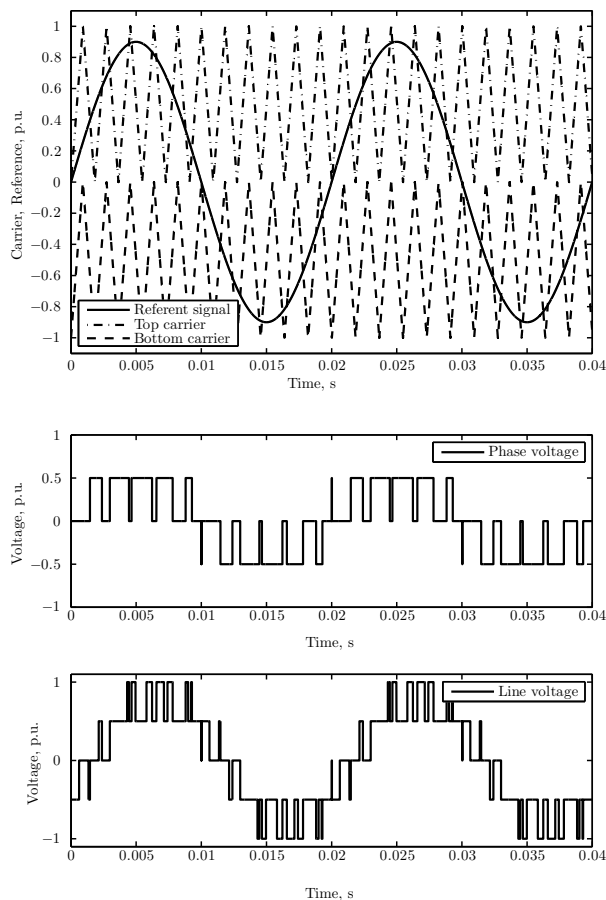


Figure 2. The concept of a three-level neutral-point clamped inverter and the output voltage waveform, $m_a = 0, 8$, $m_f = 10$

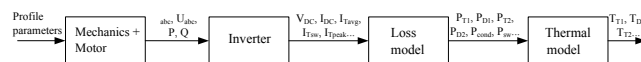


Figure 3. Block scheme of the simulation package

A. Electromechanical system simulation

Electromechanical simulation is the first part of the electric drive simulation. The input parameters for this simulation are the vehicle parameters (vehicle mass, number of engines, transmission ratios, wheel diameter, friction coefficient, ...) and the drive motor limits and parameters.

An IPM (*Interior Permanent Magnet*) motor was used as the drive motor. Table III shows the parameters that define the motor: permanent magnets flux, direct axis reactance, quadrature axis reactance, nominal current, nominal voltage and stator resistance. Picture 4 depicts the electric drive block simulation.

Table II. MAIN VEHICLE PARAMETERS

vehicle mass, $m_v = 60000$ kg	transmission ratio, $i = 7,46$
wheel diameters, $D_w = 0,66$ m	number of engines $N_m = 6$
force of fricion $F_f = 2$ kN	$v_{max} = 20 \frac{m}{s}$

Table III. IPM MOTOR MAIN PARAMETERS USED IN THE SIMULATION

$U_n = 350$ V	$L_d = 0,43$ p.u.
$I_n = 120$ A	$L_q = 1,075$ p.u.
$f_n = 58$ Hz	$\Psi_{md} = 0,602$ p.u.
$p = 2$	$R_s = 0,05$ p.u.

Either the driver or the control circuit set the stator current reference value, with the purpose of achieving the desired speed. The stator current is usually limited to both minimum and maximum values. Afterwards it's transformed to I_d and I_q components in such a way that it satisfies the condition (1). Motor thermal limits define the current limits and, in this paper, it's value is $I_l = 1,2 \cdot I_n$.

$$I_s = \sqrt{I_d^2 + I_q^2} \quad (1)$$

The IPM motor torque is calculated using (2). Equation (2) shows that part of the torque is reluctant, since L_d and L_q are different with IPM motors. It's necessary to add motor current's I_d component, in order to utilize the reluctant torque.

$$M_m = \Psi_{md} I_q + (L_d - L_q) I_q I_d \quad (2)$$

There are several ways to calculate the necessary motor current component I_d . This paper presents an implementation of the MTPA (*Maximum Torque per Amp*) trajectory solution, taken from [7]. This solution uses the reluctant torque in an optimized fashion, achieving the minimum stator current.

The MTPA algorithm is active for as long as the motor doesn't achieve the nominal voltage, after which the field weakening algorithm is turned on. This algorithm impresses (??) the I_d current component, in order to keep the nominal voltage in the above-nominal speed area. The motor torque is deteriorating in this particular case. Bolognani [8] described a similar method of controlling an internal magnet motor.

The assumption is that the I_d and I_q current regulators are ideal, e.g. the reference current value equals the value of the motor current at all times. This assumption enables a significant simplification and shortening of the electromechanical part of the simulation.

The motor torque can be calculated, with regard to the previous simplifications and with a previously defined reference current I_s . This torque is used as a parameter of the mechanical model, which calculates the vehicle velocity. The electromechanical part of the simulation can use a larger time step, since the mechanical constants are one order of value larger than the ones necessary to calculate the electrical signals. Such time steps enable a faster mechanical signal calculation.

The necessary motor inputs, currents and voltages in dq system, are transformed from abc to dq system via Park transform. The rotor angle, which is a necessary value for the transform, is obtained from the integral of the motor's angle velocity.

The implemented motor model is extremely simple, since it doesn't consider the dependence of reactances on currents, magnetizing, or the dependence of resistance on temperature, etc.

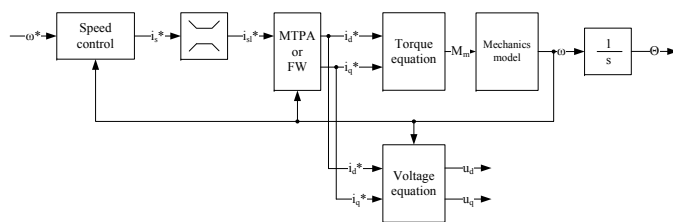


Figure 4. Block scheme of the electro-mechanic system

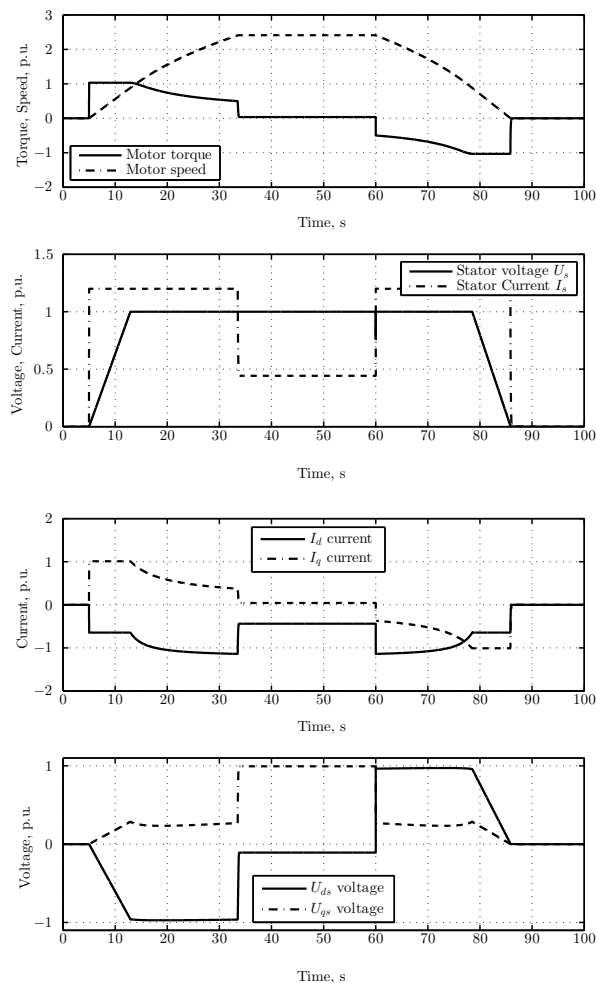


Figure 5. Torque, speed, voltage and stator current obtained from the electro-mechanic simulation

B. Electric simulation of the converter

Results of the electro-mechanic system calculus are transferred to the part of the simulation which calculates the current-voltage relations within the converter topology. Currents and voltages needed to achieve the desired shaft torque are the inputs. These currents and voltages are necessary for acquiring the values of control variables needed to control the three-level inverter and to calculate the topology's current-voltage relations. The averaged model simulation was selected based on [9], since the profile of the calculation exceeds one minute

Table IV. MAIN PARAMETERS FOR THE INVERTER USED IN SIMULATION

source voltage, $U_s = 600$ V	source resistance, $R_{DC} = 0,2 \Omega$
initial capacitor voltage $C_{DC}, U_{co} = 600$ V	capacitance $C_{DC} = 10$ mF
voltage limit, $U_{max} = 750$ V	$f_{sw} = 5$ kHz

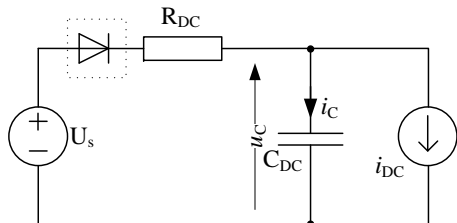


Figure 6. Equivalent circuit of DC link

(the paper uses a profile of duration of roughly 100 s).

It is important to determine the DC link voltage in order to correctly calculate the duty cycles $D_{1,2,3}$. $D_{1,2,3}$ represent control signals for all three phases of the inverter. DC link voltage change should be taken into account, since it is not a constant value. Figure 6. shows the scheme of the DC link. The current which the DC link is feeding to the inverter, i_{DC} , can be expressed through the inverter's output power. The output power can be derived from the output power of the motor P_{out} and the DC link capacitor voltage u_c as:

$$i_{DC}(t) = \frac{P_{out}(t)}{u_c(t)}. \quad (3)$$

Capacitor current can be expressed as:

$$i_c(t) = \frac{U_s - u_c(t)}{R_{DC}} - \frac{P_{out}(t)}{u_c(t)}. \quad (4)$$

At this point we can express the formula for the DC link voltage:

$$\frac{du_c(t)}{dt} = \frac{1}{C_{DC}} \left(\frac{U_s - u_c(t)}{R_{DC}} - \frac{P_{out}(t)}{u_c(t)} \right), \quad (5)$$

where C_{DC} is the total capacitance of DC link capacitors, U_s is the DC source voltage and R_{DC} is the DC source resistance. As pictured in figure 6, a diode is included in the equivalent circuit if the inverter is powered from a diode bridge, or any other source which does not enable energy feedback. In that case the first member of the equation (5) can only be positive and, hence, is limited to zero. The solution of equation (5) for the case of a diode bridge power supply is derived via Euler method and pictured in figure 7. The DC link voltage is limited to 750 V and the inverter current is fed to the braking resistor as pictured in figure 7. The correct duty cycles D_1 , D_2 and D_3 can be calculated only after the DC link voltage has been determined. This method of duty cycle calculation does not take the DC link voltages ripple into consideration.

The control signal can be divided into two signals, one of which is compared to the positive carrier signal and the other which is compared to the negative control signal, since two carrier signals and one control signal is the most common method for generating switching pulses. This is the method for obtaining six control signals instead of three; D_{1P} , D_{2P} ,

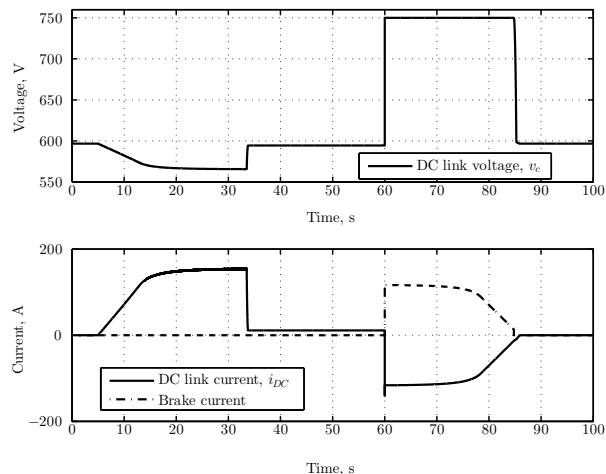


Figure 7. DC link simulation results

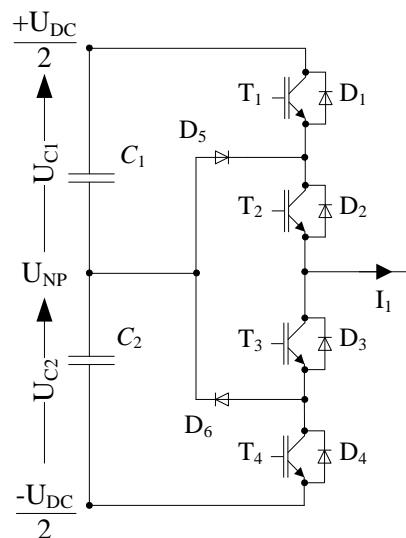


Figure 8. A three-level NPC scheme (one phase leg)

D_{3P} , D_{1N} , D_{2N} i D_{3N} , expression (6).

$$\begin{aligned} D_{1P,2P,3P} &= D_{1,2,3} \cdot (D_{1,2,3} > 0) \\ D_{1N,2N,3N} &= D_{1,2,3} \cdot (D_{1,2,3} < 0) \end{aligned} \quad (6)$$

Since all semiconductor valves used in this topology conduct current in one direction, it is necessary do divide the output current (of each leg) into two parts: positive and negative part, (7). This classification enables us to distinct the current each valve within the topology is conducting.

$$\begin{aligned} I_{1P,2P,3P} &= I_{1,2,3} \cdot (I_{1,2,3} > 0) \\ I_{1N,2N,3N} &= I_{1,2,3} \cdot (I_{1,2,3} < 0) \end{aligned} \quad (7)$$

Semiconductor valves T_1 , T_2 , D_3 , D_4 and D_5 can conduct only the positive component of the output current I_{1P} , while T_3 , T_4 , D_1 , D_2 and D_6 can conduct only the negative part I_{1N} .

The average value of current through each of the semiconductor elements can be calculated from equations (6) and

Table V. CURRENT RELATIONS EXPRESSIONS FOR ONE LEG OF THE THREE-LEVEL NPC INVERTER

	I_{avg}	I_{peak}	I_{sw}
T ₁	$I_{1P} \cdot D_{1P}$	I_{1P}	$I_{1P} \cdot (D_{1P} \in \langle 0, 1 \rangle)$
T ₂	$I_{1P} \cdot (1 - D_{1N})$	I_{1P}	$I_{1P} \cdot (D_{1N} \in \langle 0, 1 \rangle)$
D ₃	$I_{1P} \cdot D_{1N}$	I_{1P}	0, soft
D ₄	$I_{1P} \cdot D_{1N}$	I_{1P}	$I_{1P} \cdot (D_{1N} \in \langle 0, 1 \rangle)$
D ₅	$I_{1P} \cdot (1 - D_{1N} - D_{1P})$	I_{1P}	$I_{1P} \cdot (D_{1P} \in \langle 0, 1 \rangle)$
T ₄	$I_{1N} \cdot D_{1N}$	I_{1N}	$I_{1N} \cdot (D_{1N} \in \langle 0, 1 \rangle)$
T ₃	$I_{1N} \cdot (1 - D_{PN})$	I_{1N}	$I_{1N} \cdot (D_{1P} \in \langle 0, 1 \rangle)$
D ₂	$I_{1N} \cdot D_{1P}$	I_{1N}	0, soft
D ₁	$I_{1N} \cdot D_{1P}$	I_{1N}	$I_{1N} \cdot (D_{1P} \in \langle 0, 1 \rangle)$
D ₆	$I_{1N} \cdot (1 - D_{1N} - D_{1P})$	I_{1N}	$I_{1N} \cdot (D_{1N} \in \langle 0, 1 \rangle)$

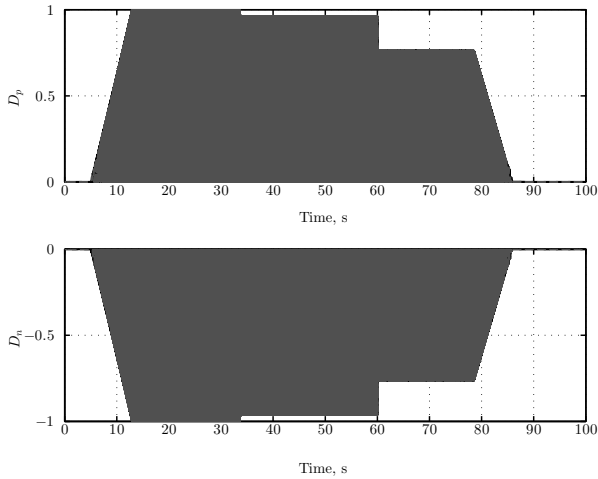


Figure 9. Duty cycles calculated scaled with the DC link voltage in case of sine modulation

(7) and the distribution of current through elements of the topology branches. E.g. element D_{1P} determines the duty cycle of the transistor T_1 . The transistor can conduct only the positive part of the current I_{1P} while on. The average value of transistor T_1 current for this case is $I_{T_{1avg}} = I_{1P} \cdot D_{1P}$. Current $I_{sw} = I_{1P} \cdot (D_{1P} \in \langle 0, 1 \rangle)$ equals the peak value of the current commuting through the same transistor (existing only when D_{1P} is in the interval between 0 and 1 i.e. when the carrier signal has the same value as the control signal) and, hence, is important to calculate the switching losses. A table containing the expressions for the average and peak values for each of the inverter leg elements from figure 8 is depicted in V. Expressions in the table were derived in a similar manner as the first transistor.

Current relations of each of the semiconductor valves within the topology can be calculated using the table V, while knowing the output currents.

Average values of the DC link currents I_p , I_n and I_{np} , pictured in figure 10, can be calculated, in case the average values of all semiconductor elements are known. Sums of currents of transistors T_{11} , T_{12} , T_{13} and diodes D_{11} , D_{12} , D_{13} can enable simplified expressions for currents I_p and I_n , as pictured in figure 1. Hence, I_p is

$$I_p = I_{1P}D_{1P} + I_{2P}D_{2P} + I_{3P}D_{3P} - I_{1N}D_{1P} - I_{2N}D_{2P} - I_{3N}D_{3P} = I_1D_{1P} + I_2D_{2P} + I_3D_{3P}, \quad (8)$$

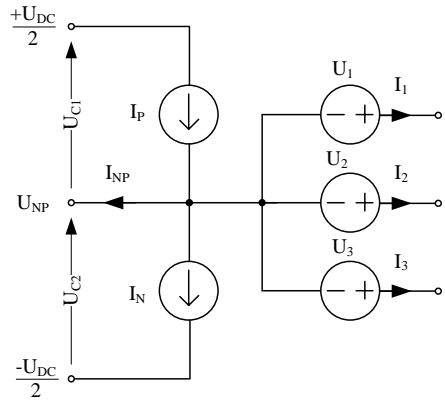


Figure 10. The averaged model of a three-level NPC inverter scheme

i.e. for I_n

$$I_n = I_{1N}D_{1N} + I_{2N}D_{2N} + I_{3N}D_{3N} - I_{1P}D_{1N} - I_{2P}D_{2N} - I_{3P}D_{3N} = I_1D_{1N} + I_2D_{2N} + I_3D_{3N}. \quad (9)$$

The current causing the neutral point voltage ripple I_{np} can be determined after the currents I_p and I_n have been determined. Third harmonic multiples are predominant in current I_{np} and are inherent for this topology [10]. With regard to figure 10., the capacitor neutral point current can be expressed as:

$$I_{np} = I_p - I_n - I_1 - I_2 - I_3. \quad (10)$$

With the assumption that the capacitors are $C_1 = C_2 = C_{uk}/2$, a shorter calculation gives the neutral point voltage ripple. The middle point voltage ripple is:

$$u_{np}(t) = \frac{1}{4C_{uk}} \int i_{np}(t)dt. \quad (11)$$

Voltage sources represent the converter's output voltages U_1 , U_2 and U_3 and, at the same time, represent the average values of phase voltages. Output voltages of each leg depend on the capacitor voltages C_1 i C_2 and on the duty cycles:

$$\begin{aligned} U_1 &= U_{C1} \cdot D_{1P} - U_{C2} \cdot D_{1N} \\ U_2 &= U_{C1} \cdot D_{2P} - U_{C2} \cdot D_{2N} \\ U_3 &= U_{C1} \cdot D_{3P} - U_{C2} \cdot D_{3N} \end{aligned} \quad (12)$$

C. Loss model of semiconductor valves simulation

The data needed to calculate each semiconductor (mostly IGBTs and diodes) total loss is obtainable once the current and voltage relations simulation within the whole topology is complete. The idea is to create a loss model where the model parameters are going to be loaded from the accessible data provided by vendors.

Most semiconductor module vendors offer various data and device characteristics in their catalogues. These can serve as parameters for loss calculation. Some of these characteristics are:

- dependency of an IGBT voltage drop on current $U_{ce} = f(I_c)$

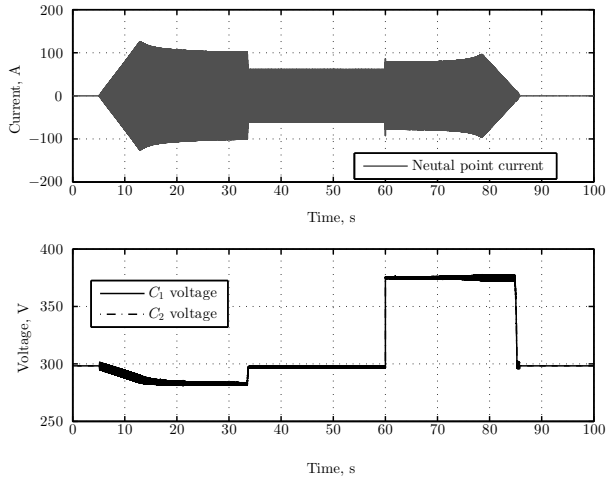


Figure 11. Results of calculus of the simulation of the neutral point current and the capacitors voltages results

- dependency of turn-on energy on current $E_{on} = f(I_c)$
- dependency of turn-off energy on current $E_{off} = f(I_c)$
- dependency of a diode voltage drop on current $U_f = f(I_D)$
- dependency of a diode recovery energy on current $E_{rr} = f(I_D)$

These characteristics are usually given in the graphic format (semiconductor datasheet). For efficient calculation it is necessary to fit the characteristics to the known function such as polynomial.

$$\begin{aligned}
 U_{ce}(I_c) &= a_0 + a_1 I_c + a_2 I_c^2 + a_3 I_c^3 + a_4 I_c^4 \\
 E_{off}(I_c) &= b_0 + b_1 I_c + b_2 I_c^2 + b_3 I_c^3 + b_4 I_c^4 \\
 E_{on}(I_c) &= c_0 + c_1 I_c + c_2 I_c^2 + c_3 I_c^3 + c_4 I_c^4 \\
 E_f(I_c) &= d_0 + d_1 I_d + d_2 I_d^2 + d_3 I_d^3 + d_4 I_d^4 \\
 E_{rr}(I_c) &= e_0 + e_1 I_d + e_2 I_d^2 + e_3 I_d^3 + e_4 I_d^4
 \end{aligned} \quad (13)$$

If switching frequency is high enough it can be assumed that the output current is constant through entire conducting interval and its value is I_{peak} and duty cycle of the observed semiconductor switch is D_n , conduction loss can be obtained using following equation.

$$\begin{aligned}
 P_{cond} &= U_{ce}(I_{peak}) \cdot I_{peak} \cdot D_n \\
 &= U_{ce}(I_{peak}) \cdot I_{avg},
 \end{aligned} \quad (14)$$

I_{avg} is average current in the switching cycle calculated from the table V.

Switching loss is calculated from the switching energies which are given with equations (13). Values of the switching energy are calculated from the polynomials and switching

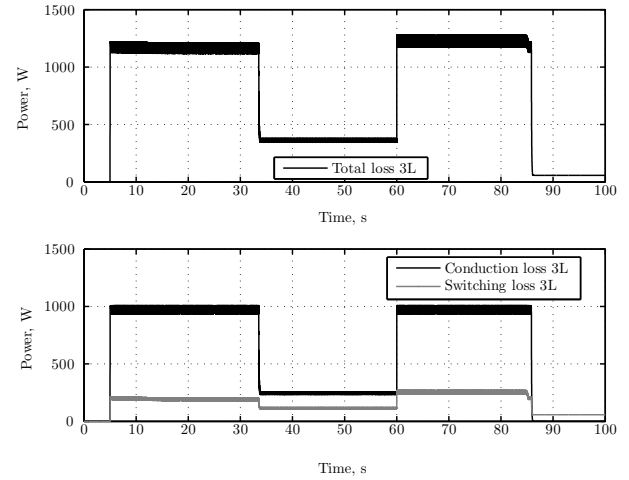


Figure 12. Result of the calculation of total loss, conduction and switching loss for three level NPC inverter obtained on the traction profile, F3L300R07PE4 power module, sine modulation, $f_{sw} = 5$ kHz

current I_{sw} , table V. Switching power loss then can be expressed as

$$\begin{aligned}
 P_{sw} &= \frac{E_{on}(I_{sw}) + E_{off}(I_{sw})}{T_{sw}} \cdot \frac{U_r}{U_{dat}} \cdot (I_{sw} > 0) \\
 &= (E_{on}(I_{sw}) + E_{off}(I_{sw})) \cdot f_{sw} \cdot \frac{U_r}{U_{dat}} \cdot (I_{sw} > 0),
 \end{aligned} \quad (15)$$

where T_{sw} represents switching period for f_{sw} , U_r blocking voltage on the device, U_{dat} blocking voltage from the datasheet and $I_{sw} > 0$ condition which shows if the observed semiconductor is switching, expression (13).

Total power loss then can be expressed as the sum of all conduction and switching loss on all semiconductors in the topology.

$$\begin{aligned}
 P_{loss} &= \sum_{i=1}^3 \sum_{j=1}^4 (P_{condT_{ij}} + P_{swT_{ij}}) + \\
 &+ \sum_{i=1}^3 \sum_{j=1}^6 (P_{condD_{ij}} + P_{swD_{ij}}).
 \end{aligned} \quad (16)$$

Figure 12. shows loss calculation for the F3L300R07PE4 power module. Loss is divided in the conduction and switching loss. It can be seen that conduction loss is dominant over the switching loss.

D. Thermal simulation of the inverter

One of the most important steps in the dimensioning of the power inverter is a calculation of the temperature rise of the semiconductors versus time. Power on the each of the semiconductors was calculated as it has been described previously. Temperature rise of the junction was calculated using thermal model described in [11]. It is important that parameters for such model can be obtained from the manufacturer data. Most of the power module manufacturers give transient thermal impedance of the semiconductor Z_{th} . Thermal impedance

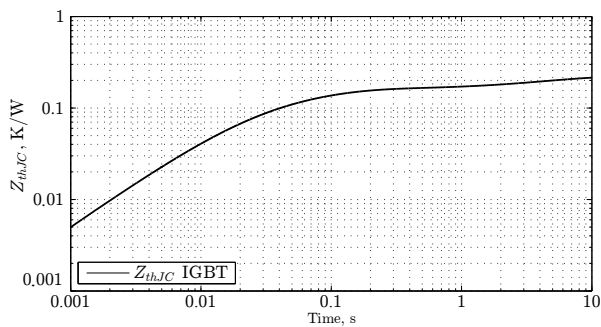


Figure 13. Transient thermal impedance of the IGBT chip in the F3L300R07PE4 power module [12]

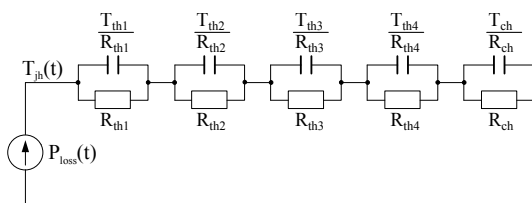


Figure 14. Simplified thermal model of the power module

can be approximated with the high order transfer function. This model can also be represented with equivalenced lumped circuit shown on figure 14.

An example of the transient thermal impedance from the manufacturer datasheet is given in the figure 13. Parameters of the lumped circuit, figure 14., can be calculated using one of the optimization techniques. Thermal model that is used in this paper is very simple and it assumes only one dimensional heat flux. Only case to junction temperature rise is taken in the consideration. Development of more detailed module is possible, but often in the early stage of the inverter design the data that is needed is not available.

IV. SIMULATION RESULTS

Final result of the traction profile simulation is switching loss in the semiconductors and temperature rise on each of the semiconductor junctions in the topology. To compare three level topology to the two level topology a simulation model of the two level inverter was build in similar manner.

Semiconductor power modules were chosen from the product portfolio of the *Infineon AG*, due to the large number of useful information in the datasheet. Lower rating module was chosen for the three level solution

- 2L module - FF450R12ME4, 400 A, 1200 V, IGBT4
- 3L module - F3L300R07PE4, 300 A, 650 V, IGBT4

A series of the simulations was conducted on the traction profile, switching frequency was varied in each instance, figure 15. The characteristics intersect at switching frequency of 3,5 kHz. Below this switching frequency two level inverter has an advantage in terms of the power loss mainly due to the lower conduction loss.

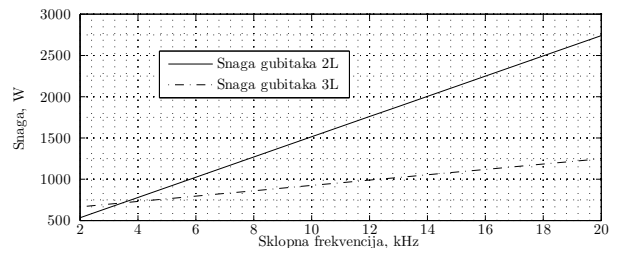


Figure 15. Average profile loss versus switching frequency for two level inverter and three level NPC inverter

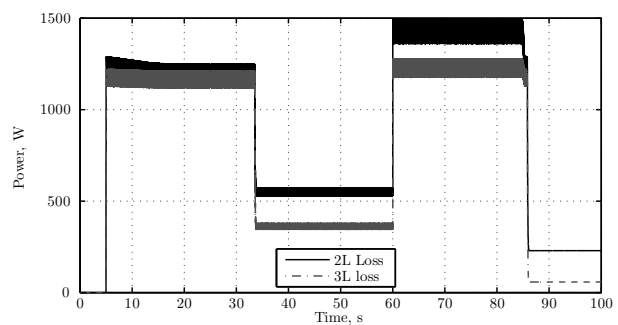


Figure 16. Comparison of the total loss of three level NPC inverter (F3L300R07PE4) and two level inverter (FF450R12ME4) at $f_{sw} = 5$ kHz

Total loss and temperature rise are compared for the identical traction profiles, figure 16., 17. i 18. Total loss of the three level inverter is lower at ($f_{sw} = 5$ kHz), figure 16. mainly due to the low switching loss, figure 17. Conduction loss in the three level topology is almost twice larger than in two level (in the three level NPC topology current is always carried trough two semiconductor devices).

Figure 18. shows temperature rise of the semiconductor junction with respect to the surface of the heatsink. Thermal resistance between case and heatsink is obtained from the module datasheet.

On the figure 18.it is possible to notice that the temperature rise on all of the semiconductors, except the NPC diode D_{51} , below 40 °C. Uneven loss distribution can be seen in the both inverter and rectifier state.

Diodes D_{5i} i D_{6i} suffer from large temperature rise during acceleration or deceleration. In these time intervals inverter operates with low voltage output and large output current. As the output voltage is low NPC diodes will conduct most of the time. Another drawback is that the fundamental frequency is lower than the thermal time constant of junction and junction temperature will follow power dissipation on the devices. Temperature rise has to be taken into an account because with high amplitude it will have influence on the lifetime of the power module. If the temperature changes are often there is a mechanical stress on the semiconductor components. This mechanical stress can lead to the destruction of the power module (desoldering, bond wire cracks etc.) [13]. This effect has to be mitigated or lowered to the acceptable value by balancing the loss between all semiconductors in the topology.

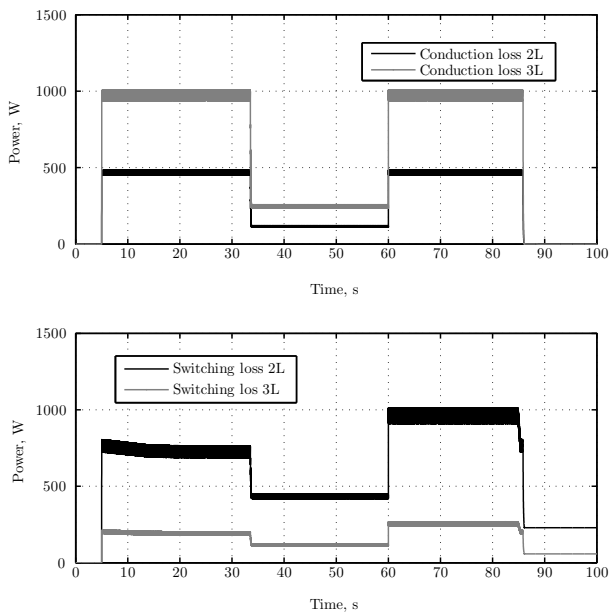


Figure 17. Loss distribution comparison 3L inverter (F3L300R07PE4) with 2L inverter (FF450R12ME4) at $f_{sw} = 5$ kHz

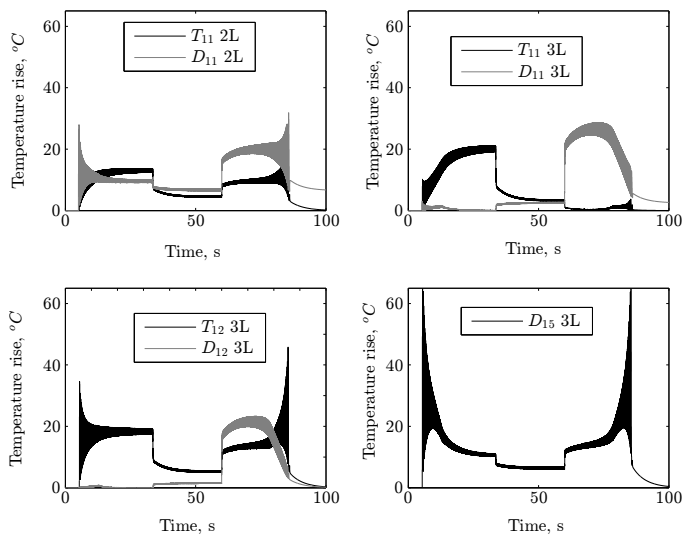


Figure 18. Temperature rise on all elements in one phase leg for 2L inverter (FF450R12ME4) and three level inverter (F3L300R07PE4) at $f_{sw} = 5$ kHz, sine modulation

There are several papers dealing with the loss balancing in the multilevel topologies [14], [15].

There are several ways to mitigate high temperature rise on the devices

- one can set output current limit with respect to the fundamental frequency (derating of the inverter at the low frequencies and DC),
- another way is to use larger power module that is capable of sinking the power dissipated on the devices

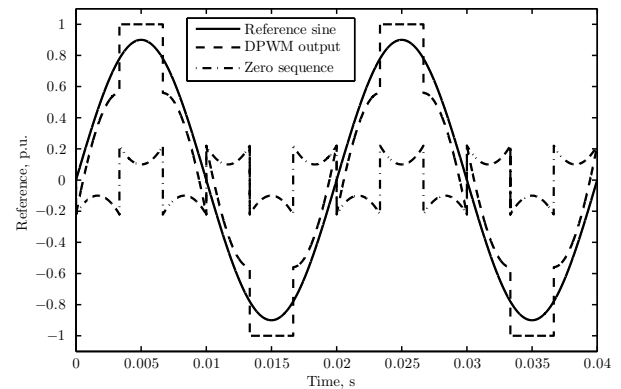


Figure 19. Discontinuous pulse width modulation DPWM

(this results in higher cost),

- and intervention on the modulation in order to balance loss between the semiconductors eg. DPWM, [16].

Discontinuous pulse width modulation (DPWM), figure 19., is used in the simulation of the entire traction profile. Results of the DPWM usage is shown on the figure 20. It can be noticed that the temperature rise on the diode D_{5i} is reduced while temperatures of the other devices are slightly increased.

It has been shown that modulation technique has an impact on the temperature distribution between the semiconductors in one phase leg. When DPWM was used, the duty cycle of 0 V output state was reduced while line to line voltage remained preserved. Reduction of the duty cycle for 0 V output state results in reduced conduction intervals for the NPC diodes which results in lower power dissipation.

Usage of different modulation technique has an influence on the neutral point current, figure 21. The increase of the neutral point current can be noticed.

This results lead to the conclusion that is necessary to research the right choice of the modulation for the each operational state (acceleration, constant speed drive, deceleration).

V. CONCLUSION

This paper gives a case study for the usage of the three level neutral point clamped inverter in the electric traction applications. Complete program support has been developed to carry out simulation of various topologies, techniques of the modulation and control laws over the traction profile. Simulation model is based on the model that is averaged on the switching period. Power loss on all semiconductors is calculated from the electrical averaged model of the topology and power loss model. Manufacturer data that is available in the common datasheets is used to calculate power loss. To calculate temperature a simple thermal model was employed. Usage of the average model, polynomial curve fits and vectorization of the calculus enabled reduction of the simulation time. Simulation time on the average PC configuration is 3 s for the traction profile with 100 s length. If the simulation is done using standard switching model, the simulation would

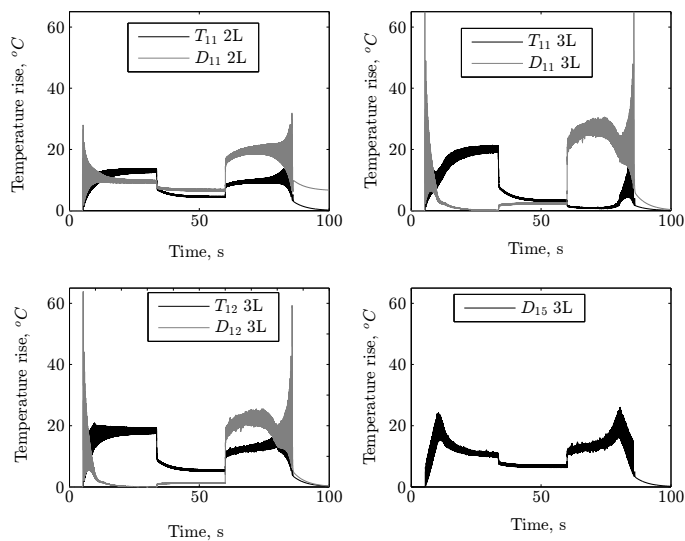


Figure 20. Temperature rise of the semiconductors for two level inverter (FF450R12ME4) and three level inverter (F3L300R07PE4) at $f_{sw} = 5$ kHz, DPWM, figure 19.

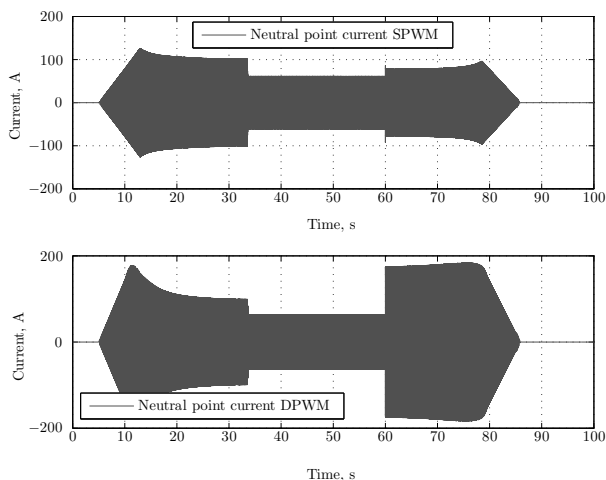


Figure 21. Neutral point current, SPWM - top, DPWM - bottom

last several hours. Fast simulation time enables usage of various optimizations; choice of the optimal semiconductor module, choice of the modulation technique, choice of passive elements, mass reduction, cost reduction etc.

From the results obtained from the simulation of the described model, it has been shown that there is a crossover frequency above which three level inverter has an advantage in terms of the lower power loss. Usage of the higher switching frequency will have an impact on lowering of the acoustic noise thus increasing comfort of the vehicle users. The effect of usage of the other modulation technique (DPWM) on the thermal balancing was discussed. Main drawbacks of this topology are: requirement for the neutral point voltage control, uneven loss distribution and higher cost.

REFERENCES

- [1] J. Rodríguez, S. Bernet, B. Wu, J. Pontt, and S. Kouro, "Multi-level voltage-source-converter topologies for industrial medium-voltage drives," *Industrial Electronics, IEEE Transactions on*, vol. 54, no. 6, pp. 2930–2945, 2007.
- [2] S. Alepuz, S. Busquets-Monge, J. Bordonau, J. Gago, D. González, and J. Balcells, "Interfacing renewable energy sources to the utility grid using a three-level inverter," *Industrial Electronics, IEEE Transactions on*, vol. 53, no. 5, pp. 1504–1511, 2006.
- [3] S. Capitaneanu, B. de Fornel, M. Fadel, and F. Jadot, "On the acoustic noise radiated by pwm ac motor drives," *Automatika*, vol. 44, no. 3-4, pp. 137–145, 2003.
- [4] S. Dieckerhoff, S. Bernet, and D. Krug, "Power loss-oriented evaluation of high voltage igbts and multilevel converters in transformerless traction applications," *Power Electronics, IEEE Transactions on*, vol. 20, no. 6, pp. 1328–1336, 2005.
- [5] R. Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications," *Industry Applications, IEEE Transactions on*, vol. 41, no. 3, pp. 855–865, 2005.
- [6] G. Holmes and T. Lipo, *Pulse width modulation for power converters: principles and practice*. IEEE press, 2003.
- [7] A. Dianov, K. Young-Kwan, L. Sang-Joon, and L. Sang-Taek, "Robust self-tuning mtpa algorithm for ipmsm drives," in *Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE*. IEEE, 2008, pp. 1355–1360.
- [8] S. Bolognani, S. Calligaro, R. Petrella, and F. Pogni, "Flux-weakening in ipm motor drives: Comparison of state-of-art algorithms and a novel proposal for controller design," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*. IEEE, 2011, pp. 1–11.
- [9] A. Yazdani and R. Iravani, *Voltage-Sourced Converters in Power Systems*. Wiley, 2010. [Online]. Available: <http://books.google.hr/books?id=XZvoeFzPchoC>
- [10] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source pwm inverters," *Power Electronics, IEEE Transactions on*, vol. 15, no. 2, pp. 242–249, 2000.
- [11] V. Blasko, R. Lukaszewski, and R. Sladky, "On line thermal model and thermal management strategy of a three phase voltage source inverter," in *Industry Applications Conference, 1999. Thirty-Fourth IAS Annual Meeting. Conference Record of the 1999 IEEE*, vol. 2. IEEE, 1999, pp. 1423–1431.
- [12] "F3L300R07PE4 data sheet, technical information," Infineon Technologies AG, 2011.
- [13] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M. Poech, "Fast power cycling test of igbt modules in traction application," in *Power Electronics and Drive Systems, 1997. Proceedings., 1997 International Conference on*, vol. 1. IEEE, 1997, pp. 425–430.
- [14] T. Bruckner and S. Bemet, "Loss balancing in three-level voltage source inverters applying active npc switches," in *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual*, vol. 2. IEEE, 2001, pp. 1135–1140.
- [15] T. Bruckner, S. Bernet, and H. Guldner, "The active npc converter and its loss-balancing control," *Industrial Electronics, IEEE Transactions on*, vol. 52, no. 3, pp. 855–868, 2005.
- [16] L. Helle, S. Munk-Nielsen, and P. Enjeti, "Generalized discontinuous dc-link balancing modulation strategy for three-level inverters," in *Power Conversion Conference, 2002. PCC Osaka 2002. Proceedings of the*, vol. 2. IEEE, 2002, pp. 359–366.